

COMPAL CONFIDENTIAL

MODEL NAME :EDC41
PCB NO :LA-G891P
BOM P/N :XXXXX

14 WHL-U UMA(non TBT)

Whiskey Lake U42


2019-02-12

REV : 1.0 (A00)

- @ : Nopop Component
- EMI@ : EMI Component
- @EMI@ : EMI Nopop Component
- ESD@ : ESDComponent
- @ESD@ : ESD Nopop Component
- RF@ : RF Component
- @RF@ : RF Nopop Component
- CONN@ : Connector Component
- DS3@ : Deep sleep support
- NDS3@ : non Deep sleep support
- CXDP@ : XDP Component
- RTD3@ : RTD Component
- NRTD3@ : RTD Component
- ST33@ : ST TPM Component
- 750@ : NUVOTON TPM Component

MB PCB	
Part Number	Description
DA8001GT000	PCB 2FB 1A-G891P REV0 MB UU NAR 1

Layout Dell logo




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REV:X00
PWB:

Power CKT : *NORTHBAY 14UU_WHL_PWR_0128
GPIO map : X10_CSLP GPIO map Rev1.3_20180529

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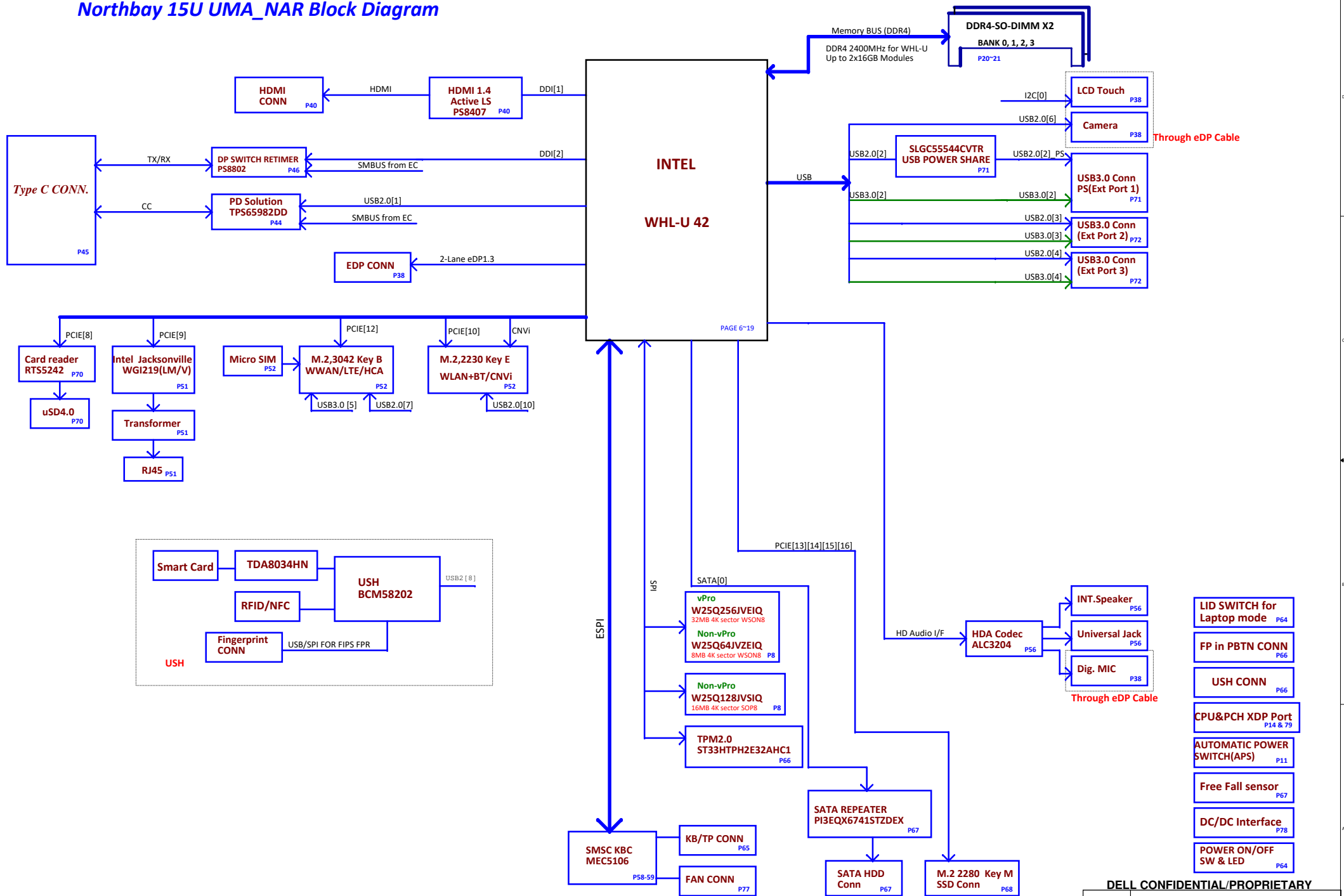
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TitleCover Sheet

SizeDocument NumberRev0.3

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Northbay 15U UMA_NAR Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S0ix/Moff	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S0ix (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB3.0	GbE	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		Type-C
USB3.0-2		PCIE-2		JUSB1
USB3.0-3		PCIE-3		JUSB2
USB3.0-4		PCIE-4		JUSB3
USB3.0-5		PCIE-5		M.2 3042(LTE)
USB3.0-6		PCIE-6		NA
		PCIE-7		
		PCIE-8		Card Reader
		PCIE-9		LOM
		PCIE-10		M.2 2230(WLAN)
		PCIE-11	SATA-0	HDD
		PCIE-12	SATA-1	M.2 3042(LTE)
		PCIE-13		
		PCIE-14		M.2 2280 SSD (PCIex4 or SATA)
		PCIE-15	SATA-1*	
		PCIE-16	SATA-2	

USB PORT#	DESTINATION
1	Type-C
2	JUSB1
3	JUSB2
4	JUSB3
5	NA
6	Camera
7	M2 3042(WWAN)
8	USH
9	FPR in PB
10	M.2 2230(BT)

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1V_PRIM	+3.3V_CV2 +1.2V_MEM +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +1.2V_RUN
S0	ON	ON	ON
S0ix	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 # 1	USB3.1 Gen1/Gen2 # 2	USB3.1 Gen1/Gen2 # 3	USB3.1 Gen1/Gen2 # 4	USB3.1 Gen1/Gen2 # 5	USB3.1 Gen1/Gen2 # 6	PCIE* # 7	PCIE* # 8	PCIE* # 9	PCIE* # 10	PCIE* # 11	PCIE* # 12	PCIE* # 13	PCIE* # 14	PCIE* # 15	PCIE* # 16
	PCIE* # 1	PCIE* # 2	PCIE* # 3	PCIE* # 4	PCIE* # 5	PCIE* # 6	GbE	GbE	GbE	SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2	
Intel® RST Support	No Support				No Support				Yes				Yes			

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Port assignment

LA-G891P



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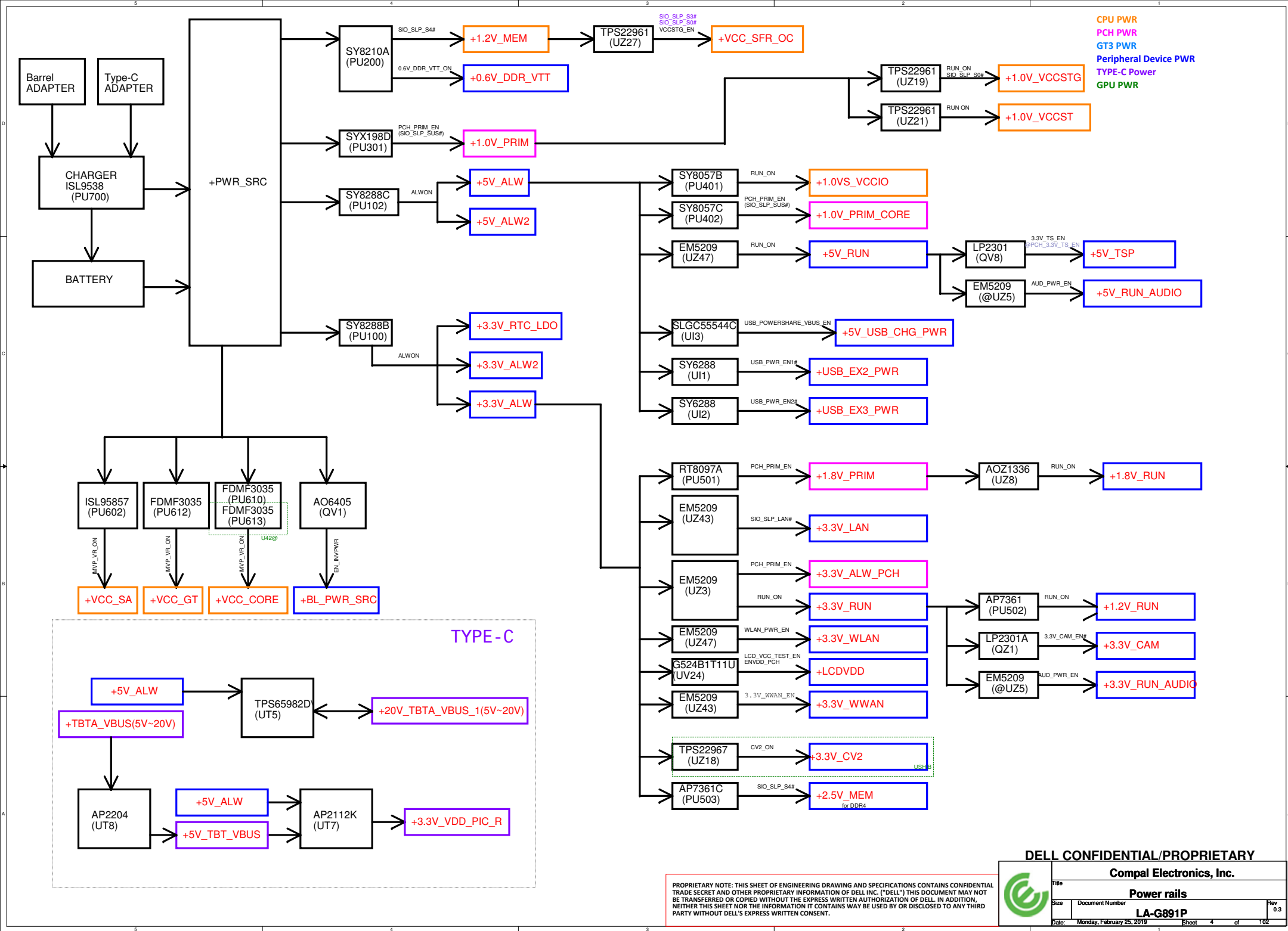
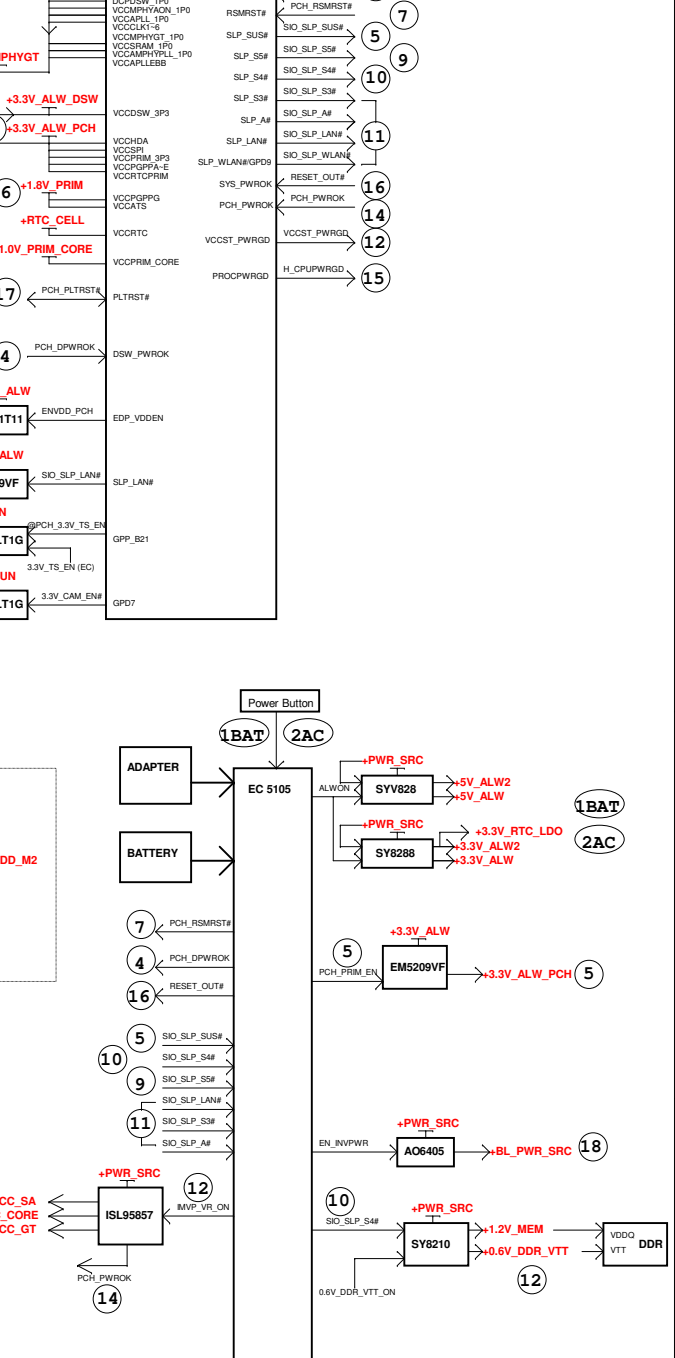




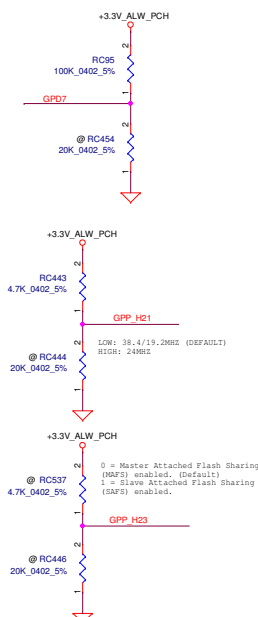
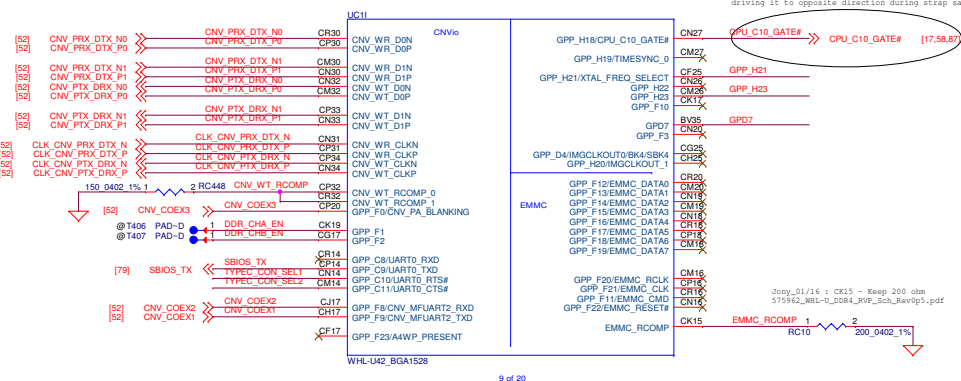
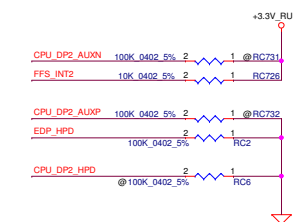
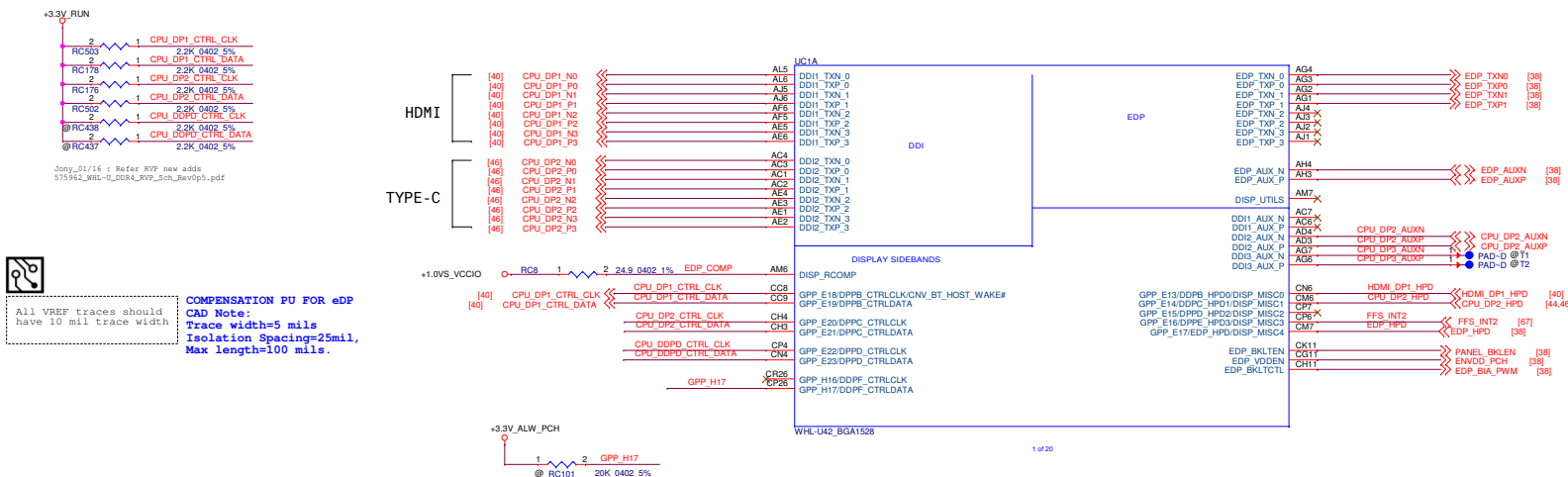
Figure 10 shows the PCH PWRBTN# connection. The PCH block has three pins: VCCPRIM_1P0, VCCPRIM_CORE, and PWRBTN#. A +1.0V PRIM source is connected to VCCPRIM_1P0. The PWRBTN# pin is connected to a signal source labeled SIO_PWRBTN# with a circled 8 next to it.



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	File _____		
	Power Sequence		
	Size _____	Document Number _____	Rev 0.3
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	File			Power Sequence			Rev
	Size	Document Number		LA-G891P			0.3
	Date:	Monday, February 25, 2019		Sheet	5	of	102

For 2LANE EDP



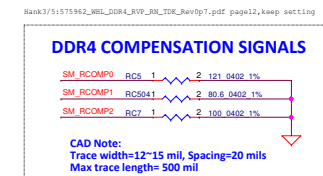
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TYPEC_CON_SEL1	LOW	LOW	HIGH	HIGH
TYPEC_CON_SEL2	LOW	HIGH	LOW	HIGH

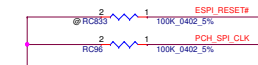
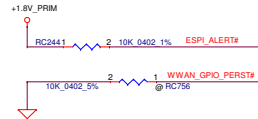
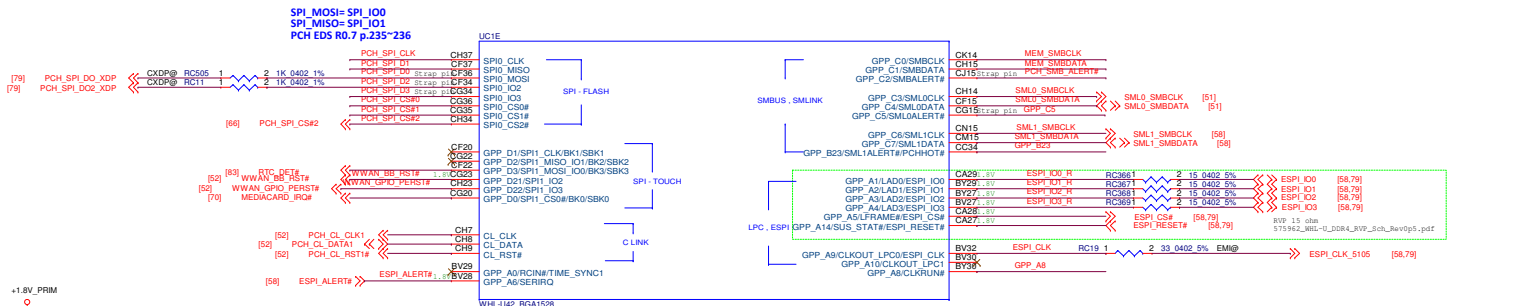
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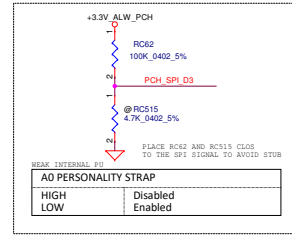
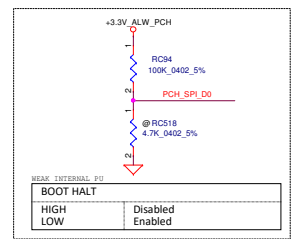
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Title			
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Size	Document Number		Rev
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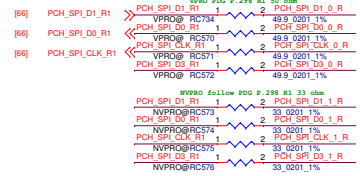


For signal deglitch, refer to 575412_WHL_U_PDG rev0p8

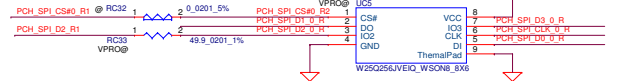


566439_CNL_PCH_UY_EDS_Vol.1_Rev.1.1.pdf
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

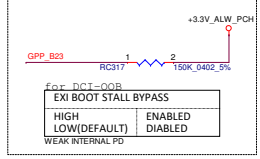
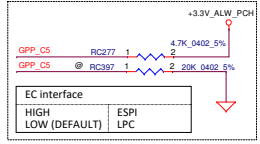
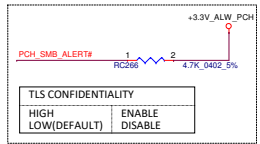
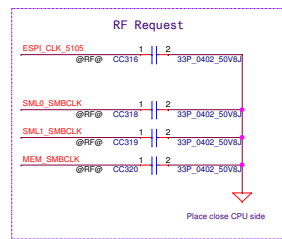
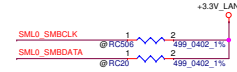
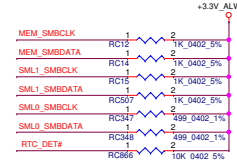
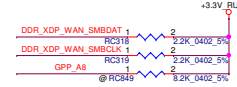
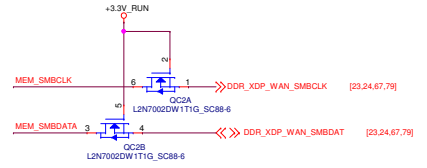
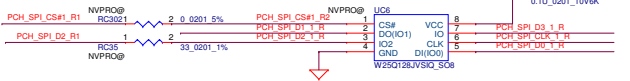
SOFTWARE TAA



For vPro 32MB WSON8 Flash ROM For Non-vPro 8MB WSON8 Flash ROM



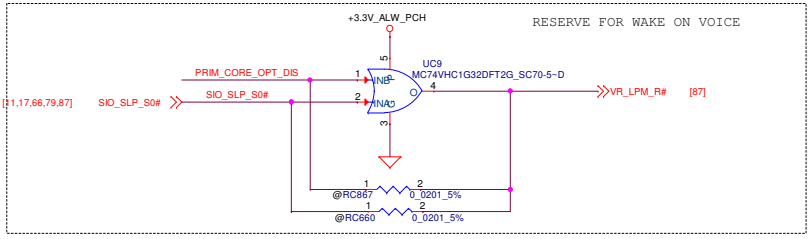
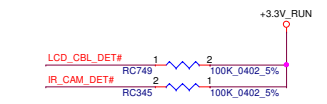
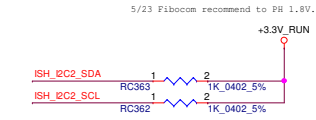
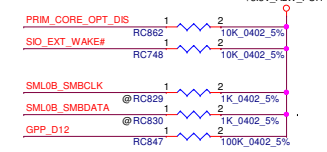
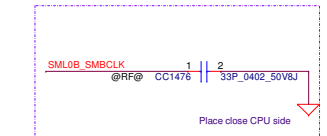
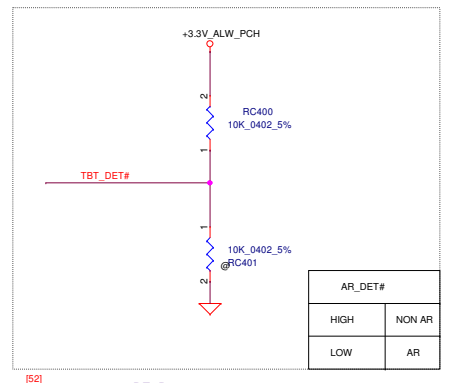
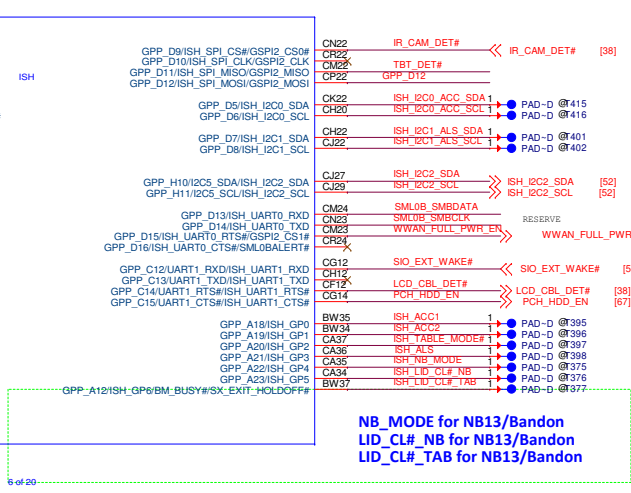
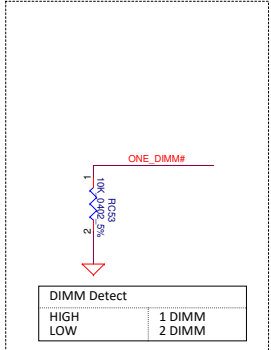
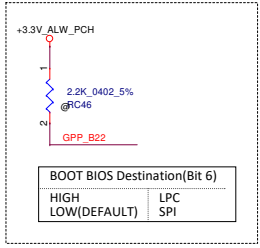
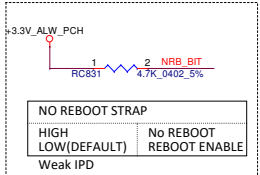
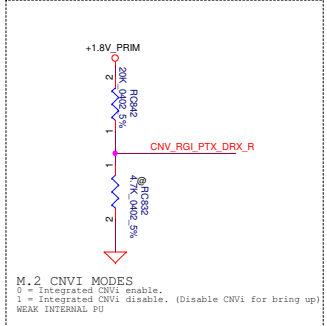
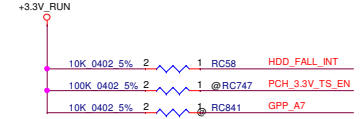
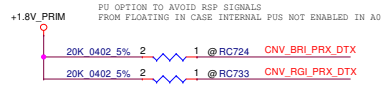
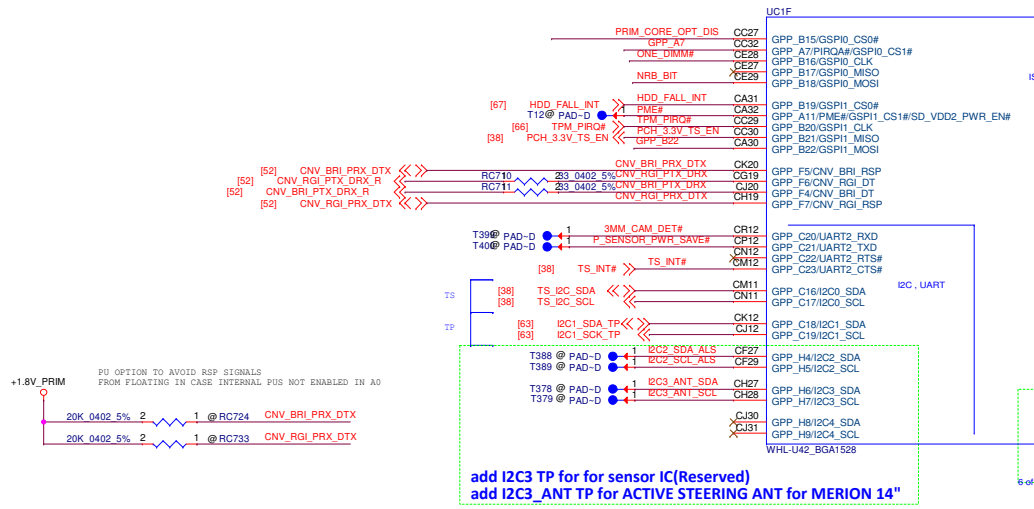
For Non-vPro 16MB SOP8 Flash ROM



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P09-MCP(314)/SPI,SMB,LPC	
LA-G891P	
Date: Monday, February 25, 2019	Sheet 8 of 102

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Size: Document Number

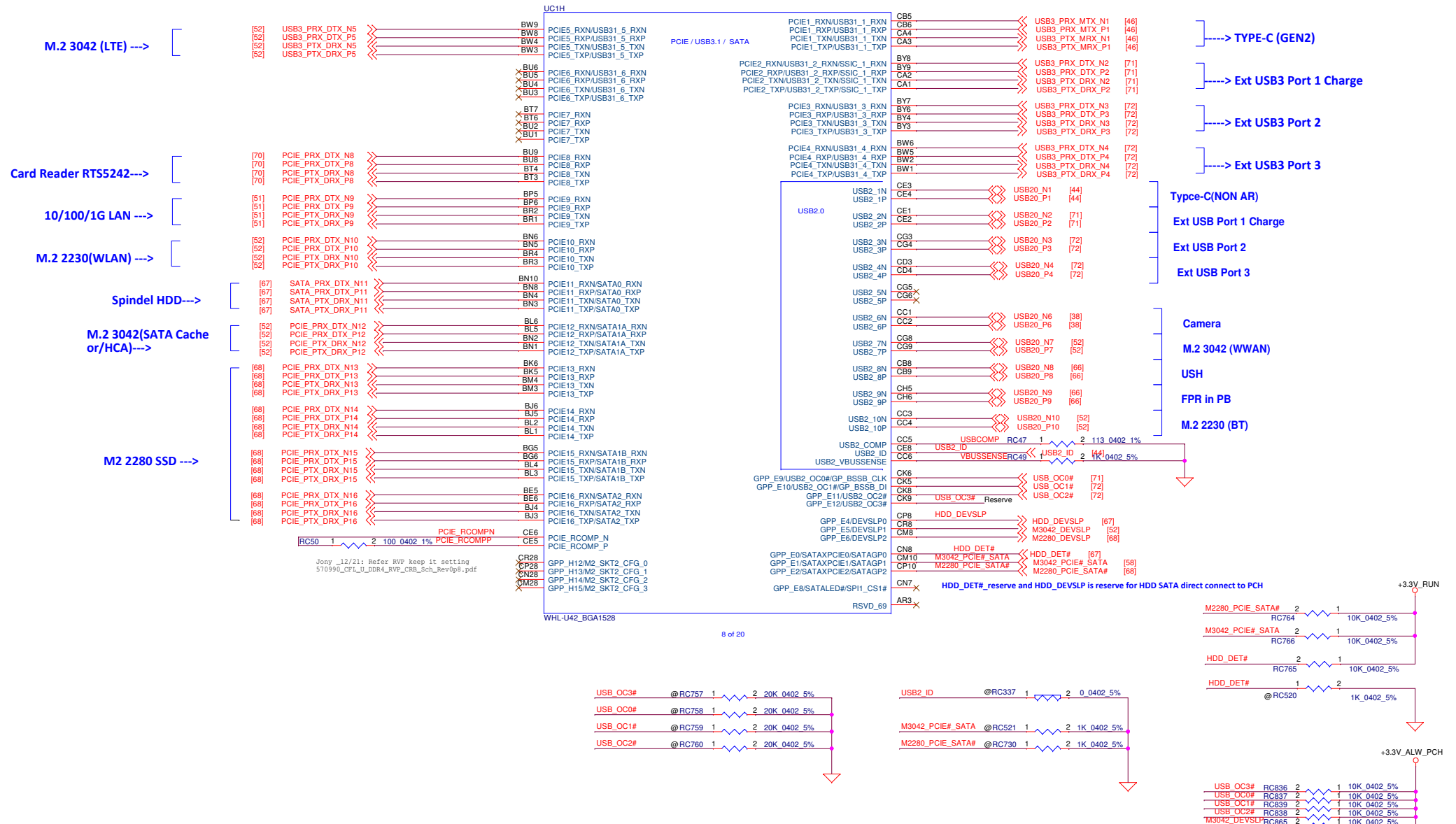
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AR,NB_Bandon DSC(follow WHL 180306C port map)

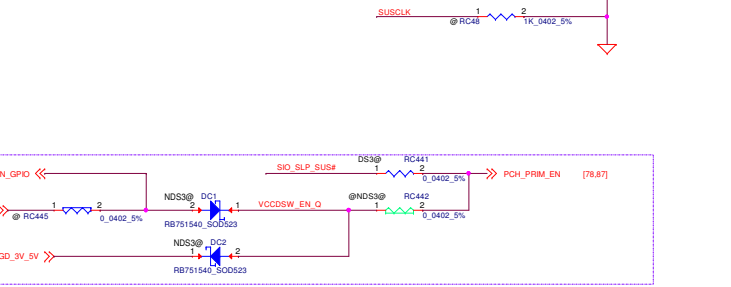
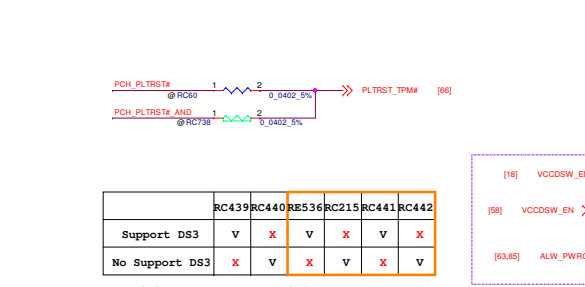
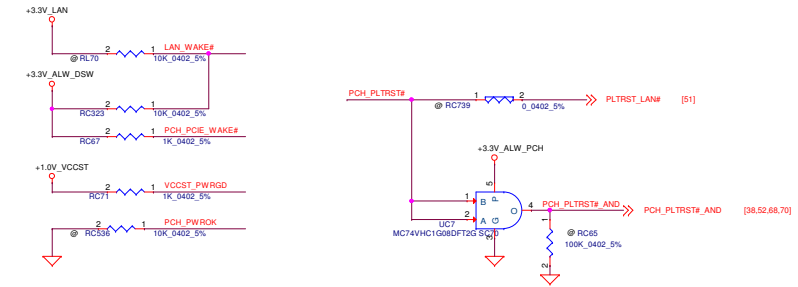
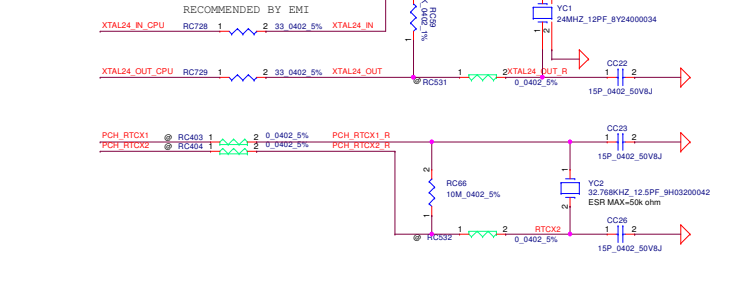
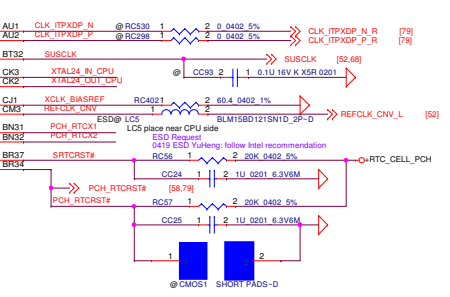
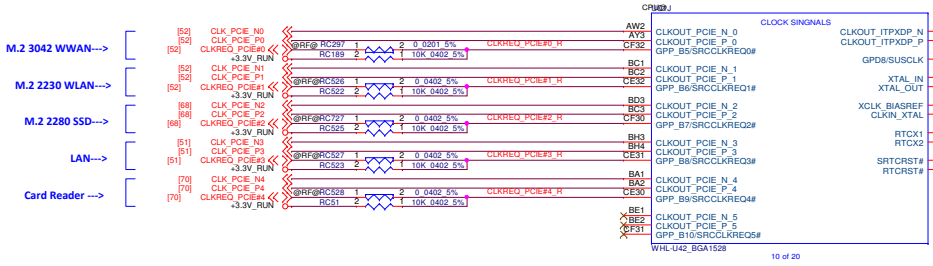


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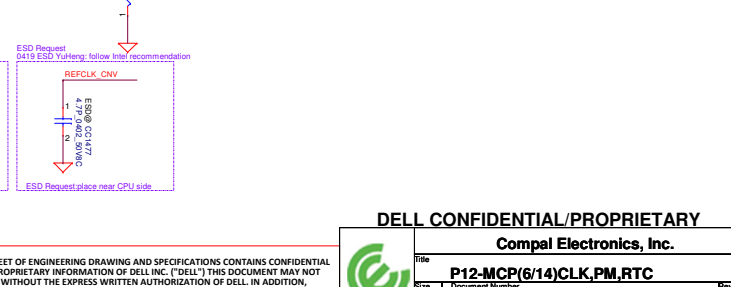
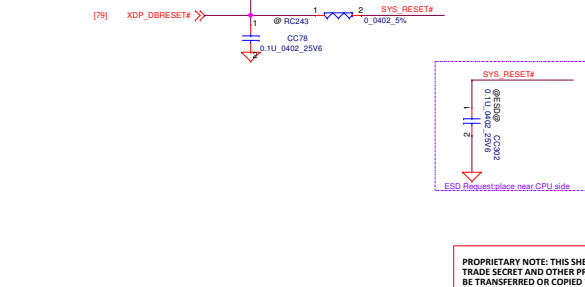
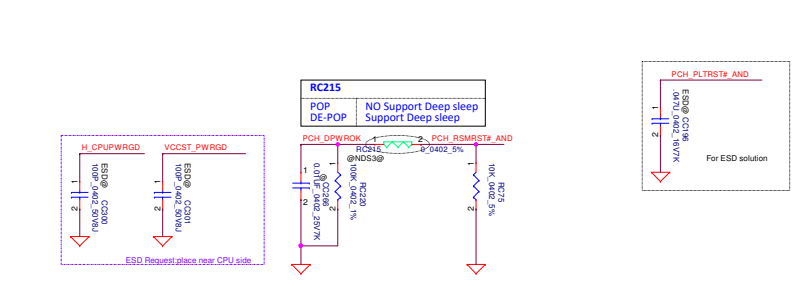
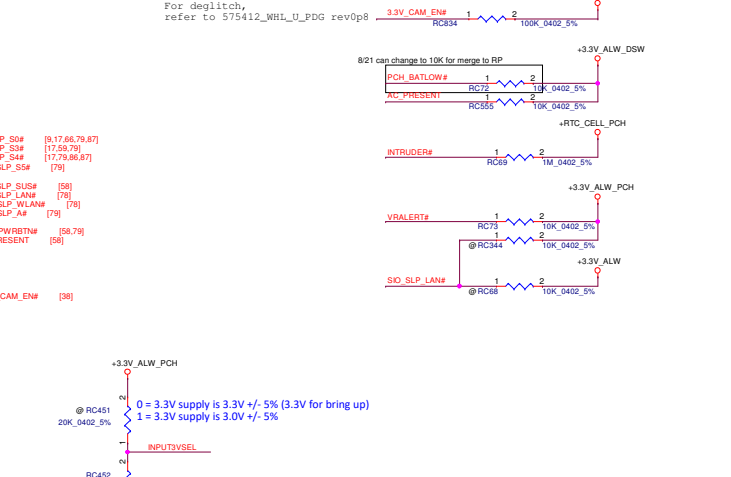
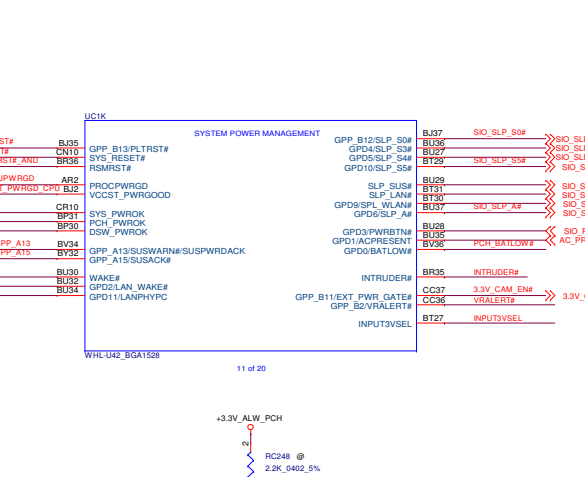
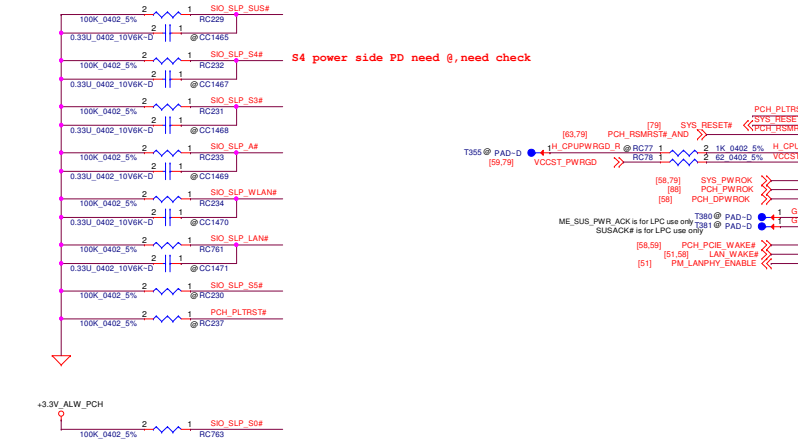


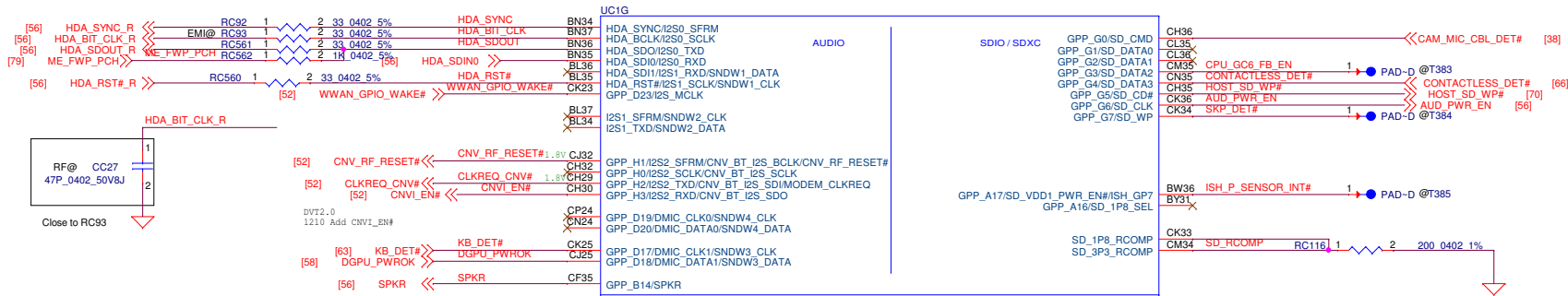
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Size	Document Number LA-G891P
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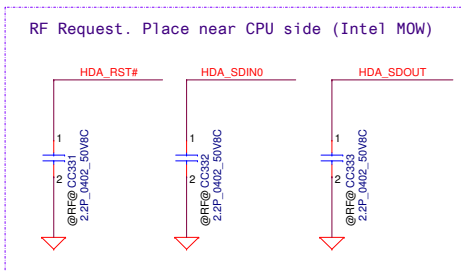
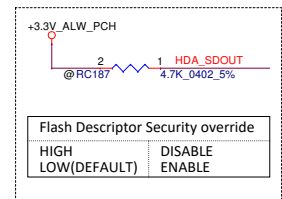
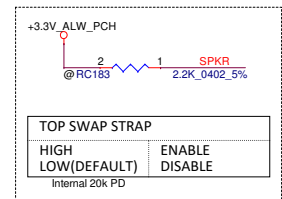
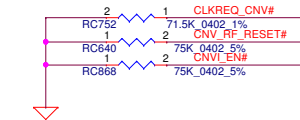
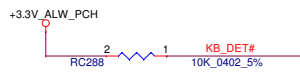
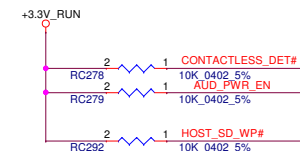
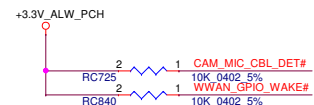


PCH GLITCH ISSUE MITIGATION(PDG p.130)





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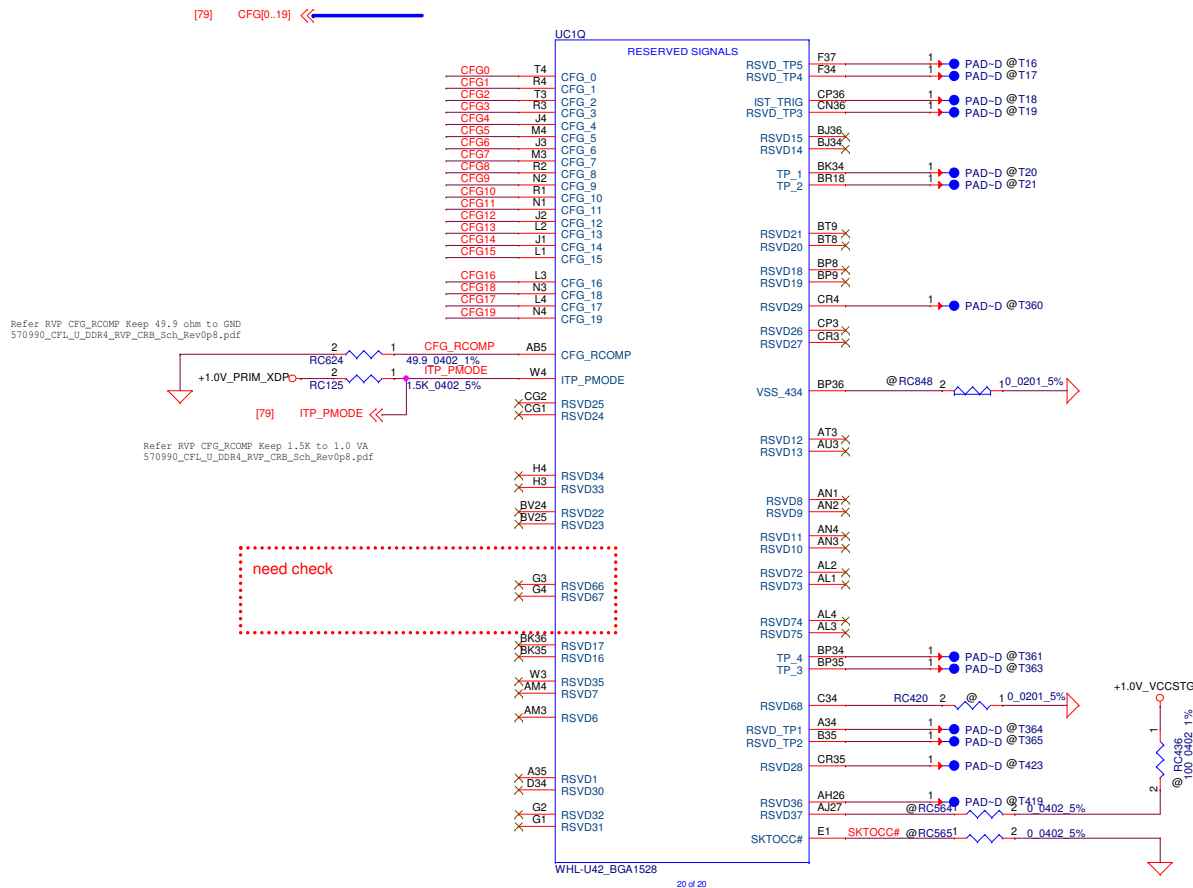
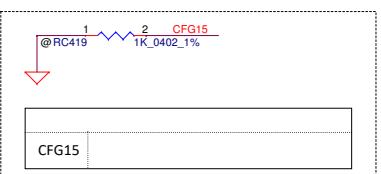
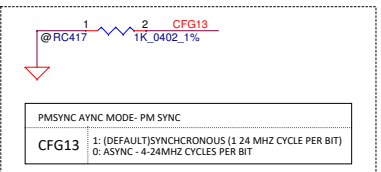
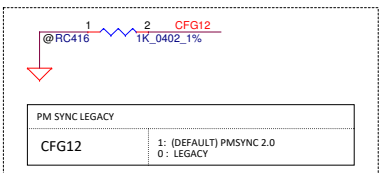
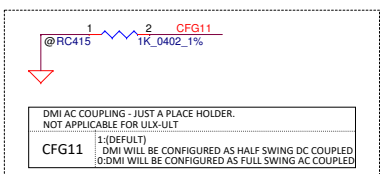
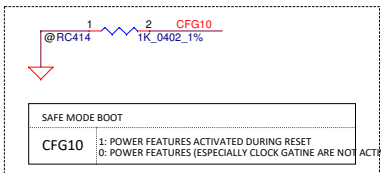
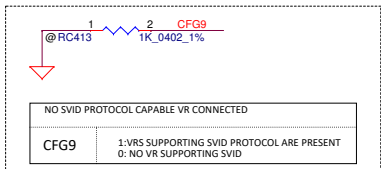
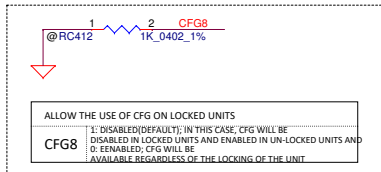
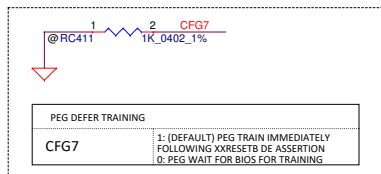
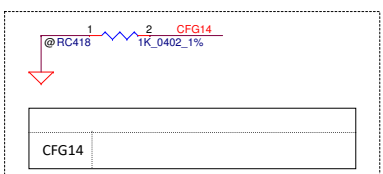
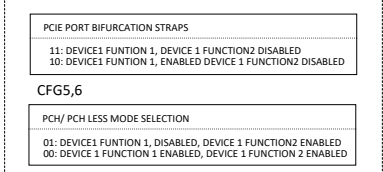
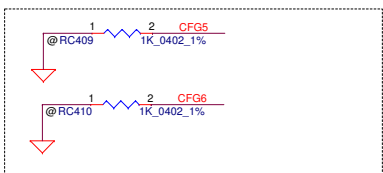
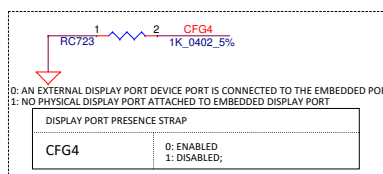
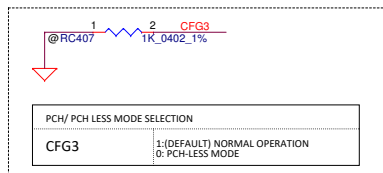
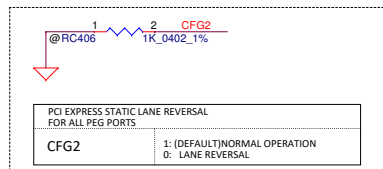
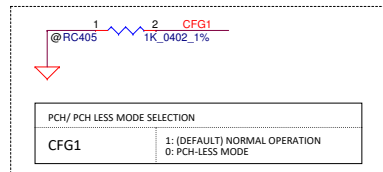
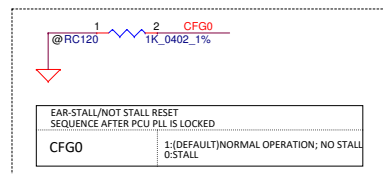
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Compal Electronics, Inc.

Title	P13-MCP(7/14)MISC,JTAG,HDA,SDIO		
Size	Document Number	LA-G891P	Rev 0.3
Date:	Monday, February 25, 2019	Sheet 12	of 102

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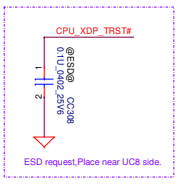
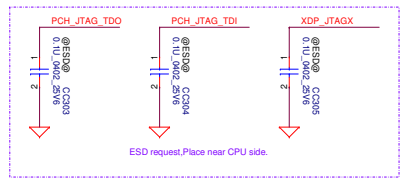
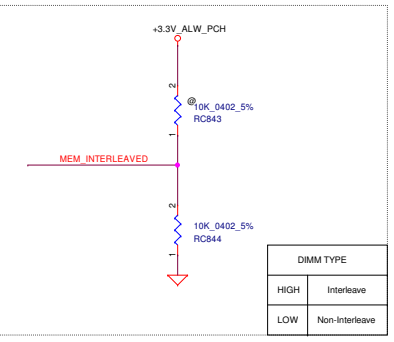
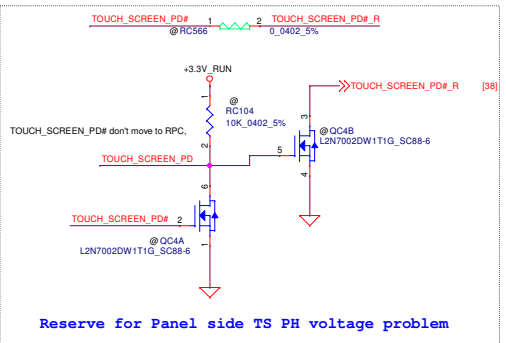
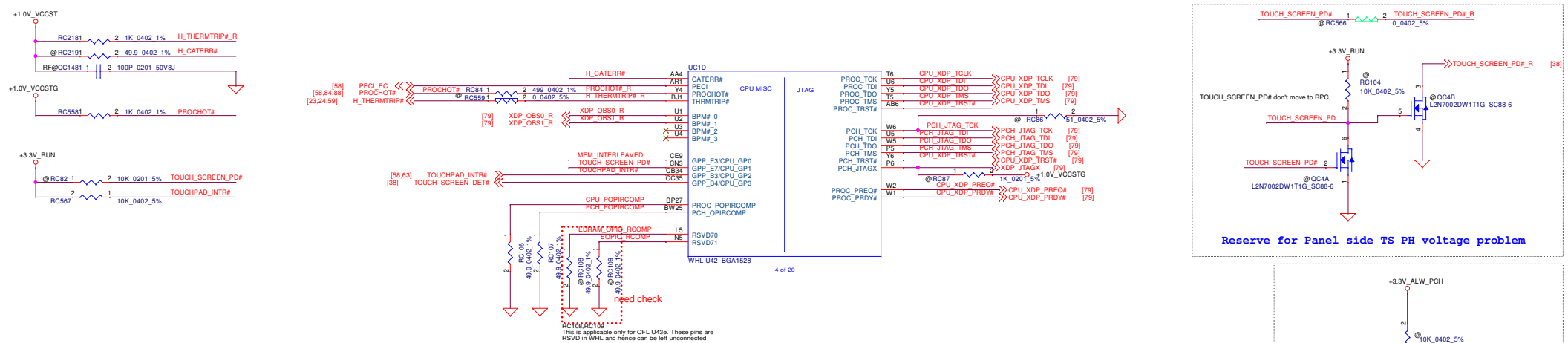
Compal Electronics, Inc.

P14-MCP(8/14)CFG.RSVD

LA-G891P

Rev	0
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Date: Monday, February 25, 2019 Sheet 13 of 102



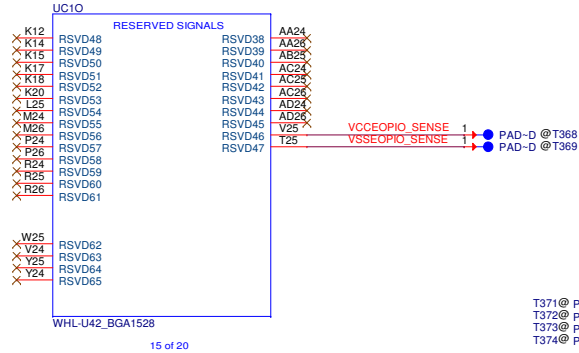
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

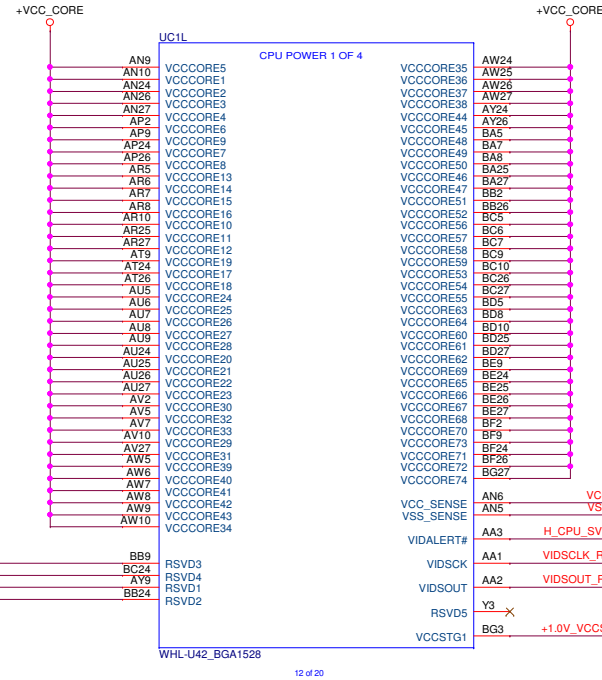
+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A

+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EOPIO: 0.8~1V, 2A - REMOVE

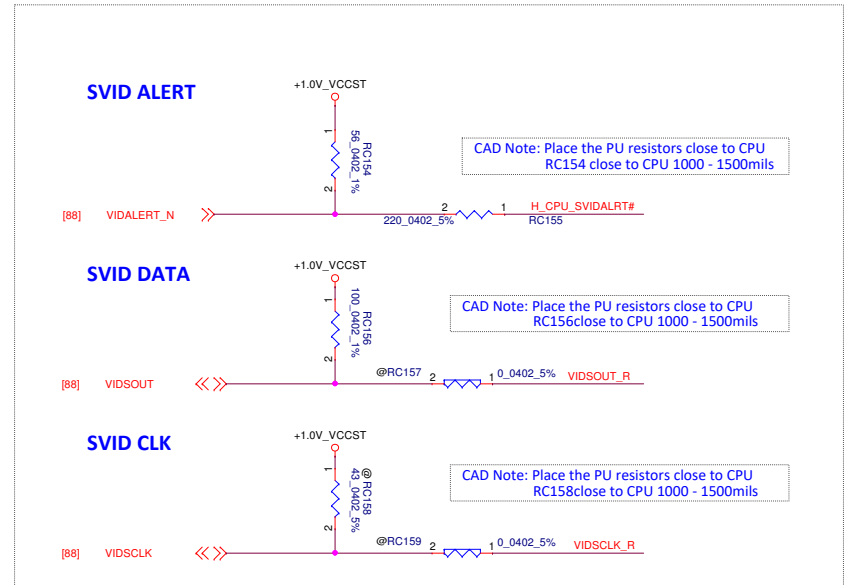
Pin Number	ICFL U43#	WHL U42 Q5/Production	CNL U22/WHL U42 E50/A
AH26	ZV#	RSVD	RSVD
T25	VSS_EOPIO_SENSE	RSVD	RSVD
V25	VCC_EOPIO_SENSE	RSVD	RSVD
AA24	VCC_EOPIO	RSVD	RSVD
AA26	VCC_EOPIO	RSVD	RSVD
AB25	VCC_EOPIO	RSVD	RSVD
AC24	VCC_EOPIO	RSVD	RSVD
AC25	VCC_EOPIO	RSVD	RSVD
AD24	VCC_EOPIO	RSVD	RSVD
AD26	VCC_EOPIO	RSVD	RSVD
K12	VCCOPC	RSVD	RSVD
K14	VCCOPC	RSVD	RSVD
K15	VCCOPC	RSVD	RSVD
K17	VCCOPC	RSVD	RSVD
K18	VCCOPC	RSVD	RSVD
K20	VCCOPC	RSVD	RSVD
L25	VCCOPC	RSVD	RSVD
M24	VCCOPC	RSVD	RSVD
M26	VCCOPC	RSVD	RSVD
P24	VCCOPC	RSVD	RSVD
P26	VCCOPC	RSVD	RSVD
R24	VCCOPC	RSVD	RSVD
R25	VCCOPC	RSVD	RSVD
R26	VCCOPC	RSVD	RSVD
K20	VCCOPC	RSVD	RSVD
L25	VCCOPC	RSVD	RSVD
M24	VCCOPC	RSVD	RSVD
M26	VCCOPC	RSVD	RSVD
P24	VCCOPC	RSVD	RSVD
P26	VCCOPC	RSVD	RSVD
R24	VCCOPC	RSVD	RSVD
R25	VCCOPC	RSVD	RSVD
R26	VCCOPC	RSVD	RSVD
Y24	VCC_OPC_1P8	RSVD	RSVD
Y25	VCC_OPC_1P8	RSVD	RSVD
Y26	VCC_OPC_1P8	RSVD	RSVD
W25	VCC_OPC_1P8	RSVD	RSVD
AU27	MSM#	RSVD	RSVD
G4	VSS	RSVD	RSVD
G3	VSS	RSVD	RSVD
G34	VSS	RSVD	RSVD



T371@ PAD-D 1 +VCC_CORE_G0
T372@ PAD-D 1 +VCC_CORE_G1
T373@ PAD-D 1 +VCC_CORE_G2
T374@ PAD-D 1 +VCC_CORE_G3



VCCOPC,VCCOPC_1P8,VCC_EOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



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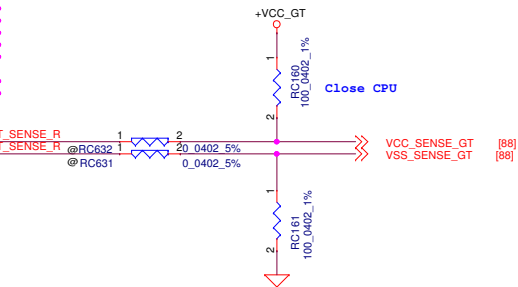
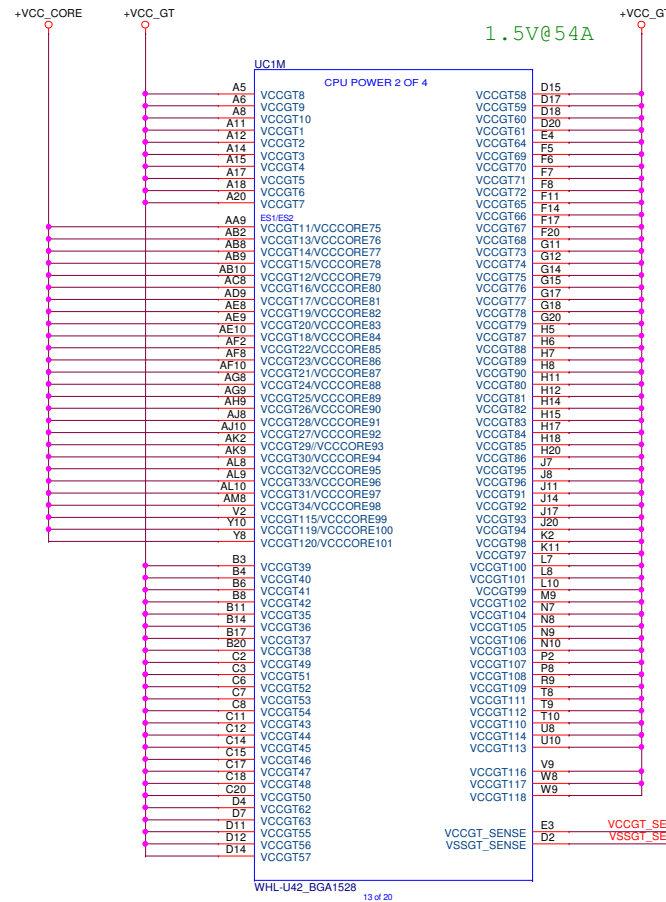
Compal Electronics, Inc.			
Title			
P16-MCP(10/14)PWR-VCC CORE			
Size	Document Number	Rev	0.3
LA-G891P			
Date	Monday, February 25, 2019	Sheet	15 of 102

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THE BALLOUT ONLY FOR WHL ES2 CPU

+VCCGT: 0.55~1.5V, 54A
+VCCGTx : 0.55~1.5V, 7A

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



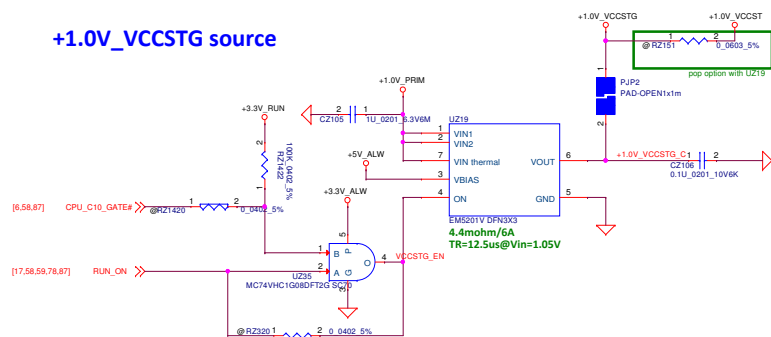
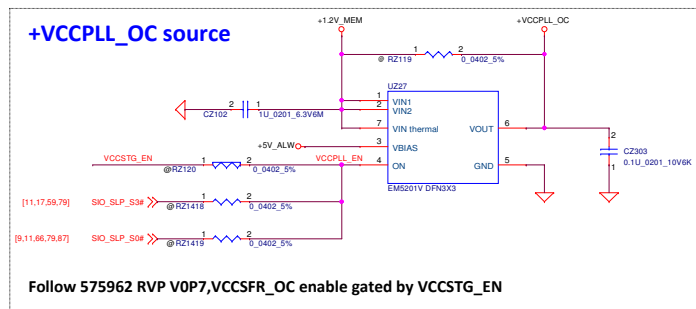
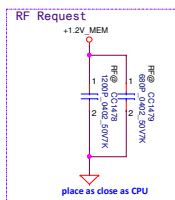
DELL CONFIDENTIAL/PROPRIETARY



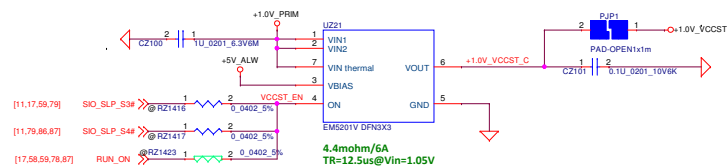
Compal Electronics, Inc.			
Title	P17-MCP(11/14)PWR-VCCGT		
Size	Document Number	Rev	0.3
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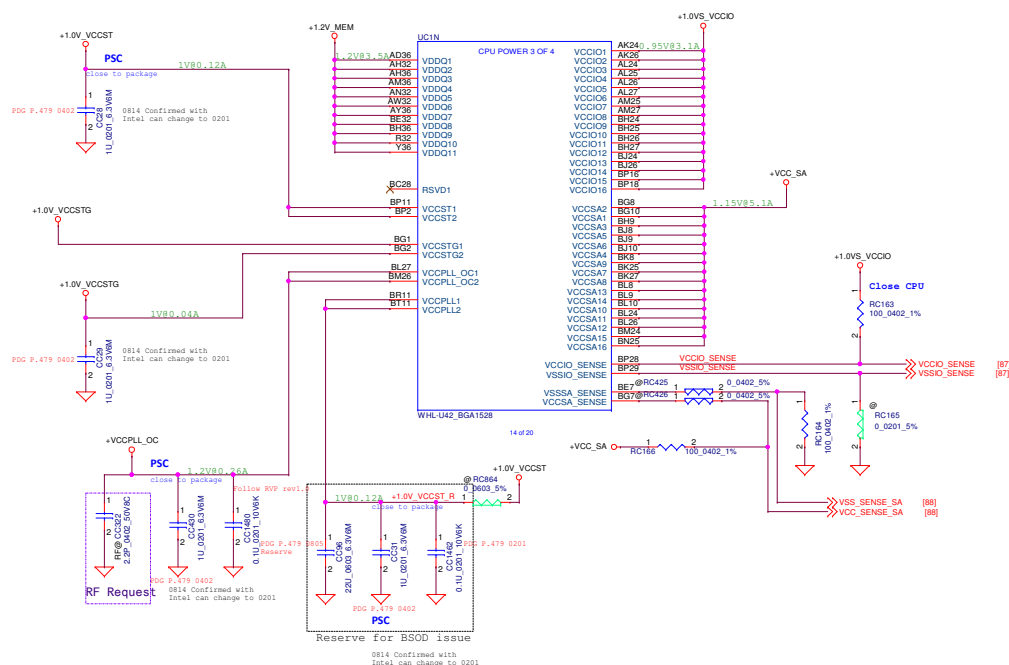
+1.2V_DDR: 1.2V, 3.5A
+1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
+1.0V_VCCSTG: 1V, 40mA
+VCCPLL_OC: 1.2V, 260mA
+1.0VS_VCCIO: 0.85~0.95V, 3.1A
+VCC_SA: 1.15V, 5.1A



Follow 575962 RVP V0P7,VCCSTG RAIL design



Follow 575962 V0p7 PDG page519,Premium design Vccst gated by RUN_ON



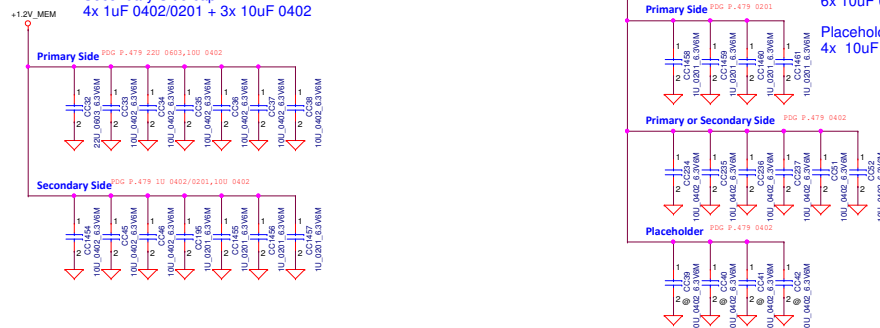
WHL_U PDG rev0.8 P.479
VDDQ:
Primary Side cap
1x 22uF 0603 + 6x 10uF 0402

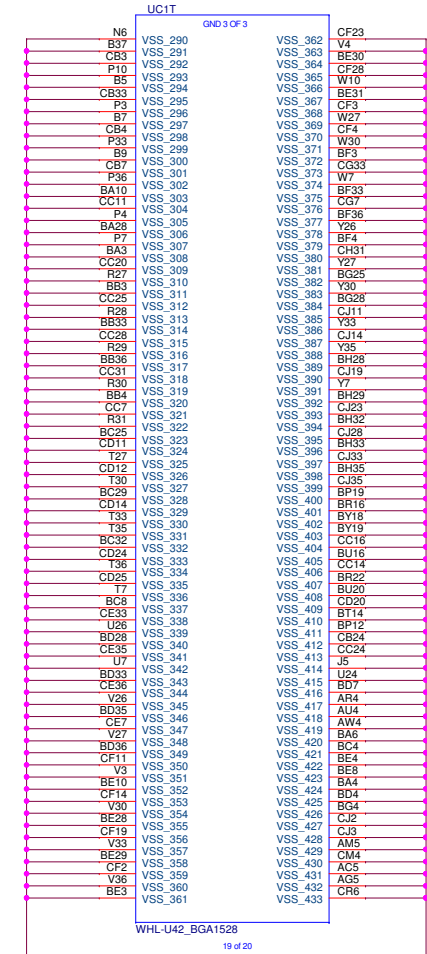
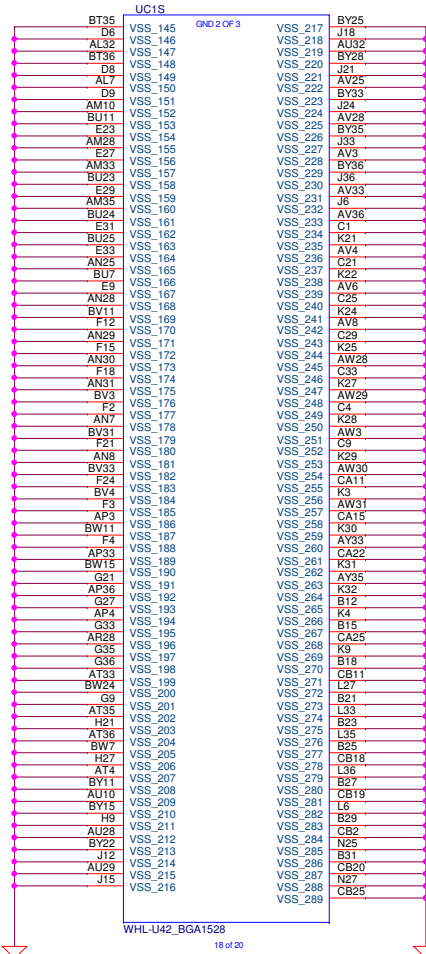
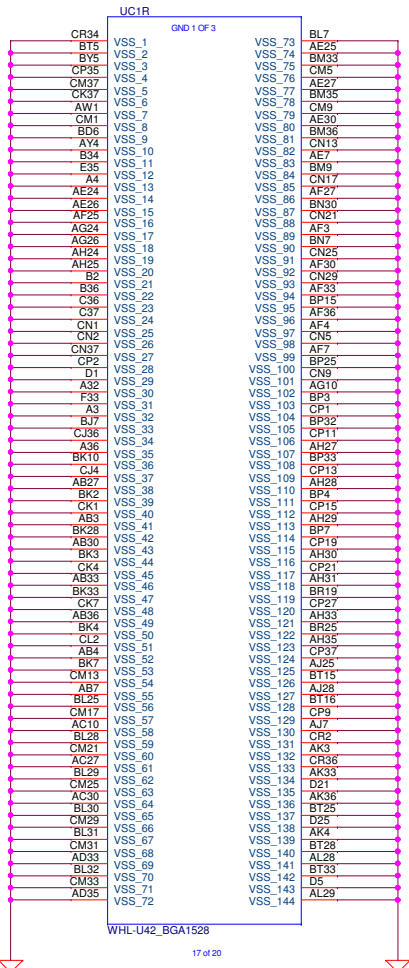
Secondary Side cap
4x 1uF 0402/0201 + 3x 10uF 0402

WHL_U PDG rev0.8 P.479
VCCIO:
Primary Side cap
4x 1uF 0201

Primary or Secondary Side
6x 10uF 0402

Placeholder Only
4x 10uF 0402





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P20-MCP(14/14)VSS

LA-G891P

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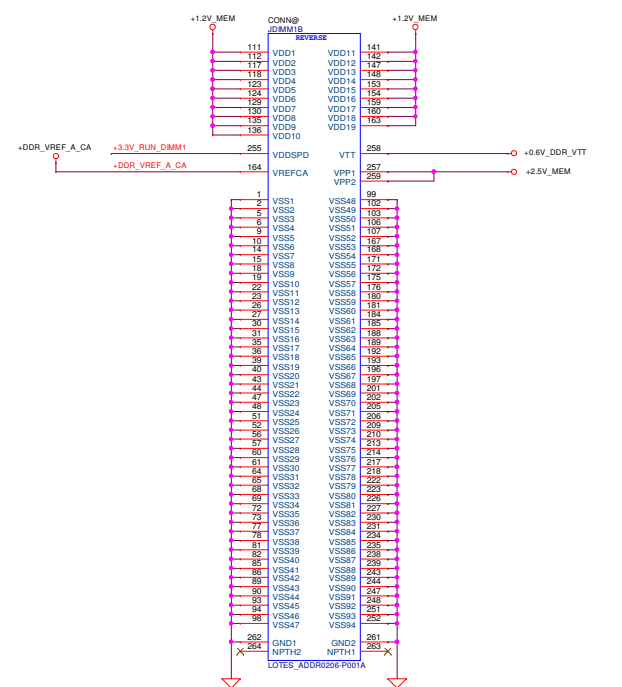
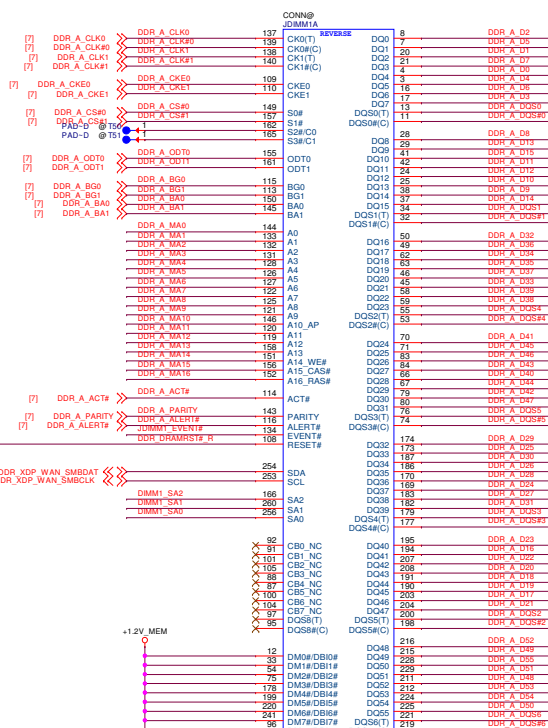
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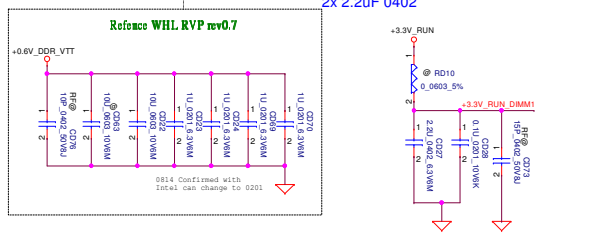
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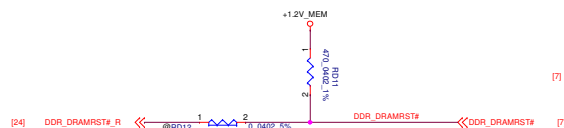
Link LOTES_ADDR0206-P001A02 done 0410



WHL_U PDG rev0.8 P.92
VTT:
Place on VTT plane close to SODIMM
2x 10uF 0603(1 cap stuffed, 1 placeholder)
4x 1uF 0402
VDDSPD:
Place close to DIMM
2x 0.1uF 0402
2x 2.2uF 0402



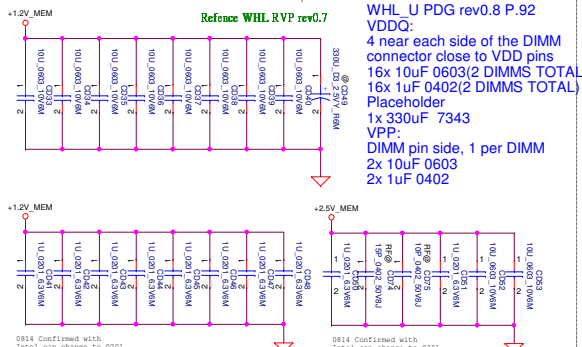
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



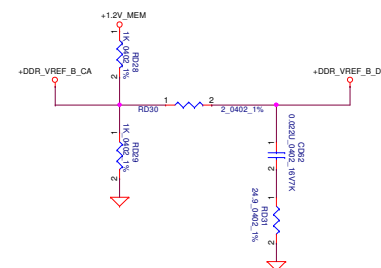
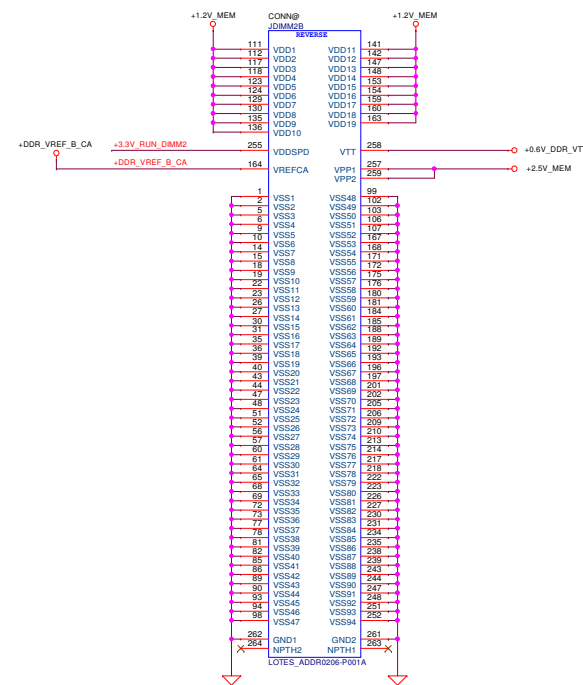
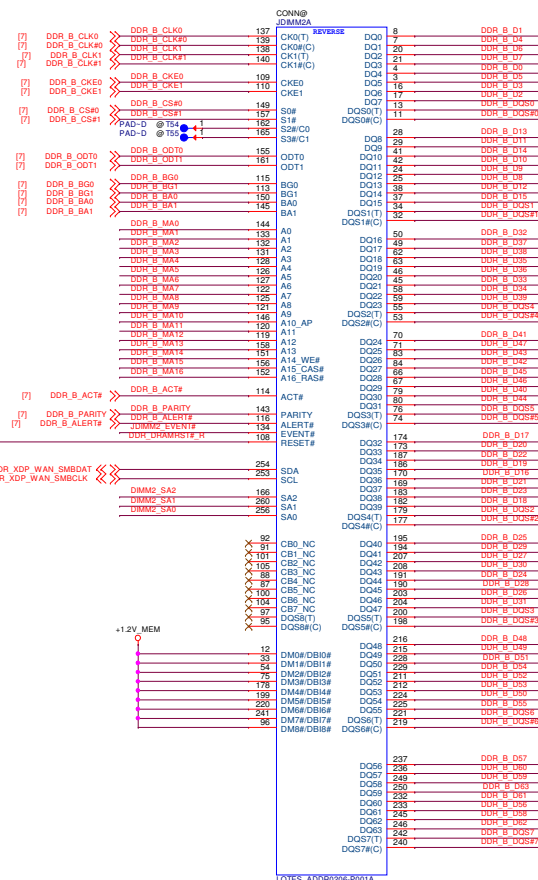
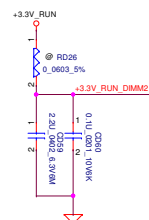
6/8 Change to SA00007WE00 DII

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[7] DDR_B_DQS#[0..7] <<>>
[7] DDR_B_D[0..63] <<>>
[7] DDR_B_DQS[0..7] <<>>
[7] DDR_B_MA[0..16] >>>
```

Reference WHL RVP rev0.7



WHL_U PDG rev0.8 P.92
VTT:
Place on VTT plane close to SODIMM
2x 10uF 0603(1 cap stuffed, 1 placeholder)
4x 1uF 0402
VDDSPD:
Place close to DIMM
2x 0.1uF 0402
2x 2.2uF 0402



Date: Monday, February 25, 2019

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Title		
DDR		
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DDR		
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DGPU		
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VRAM		
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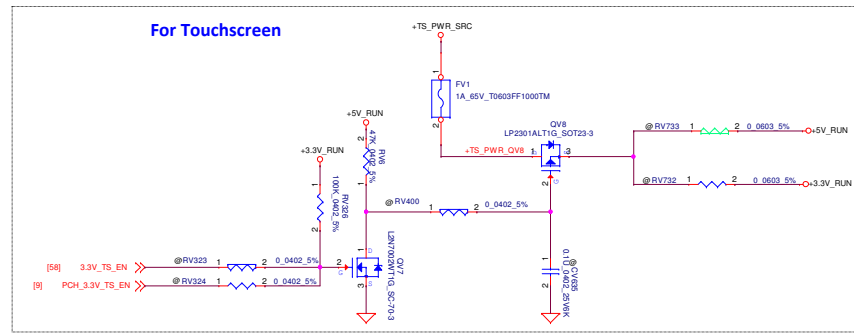
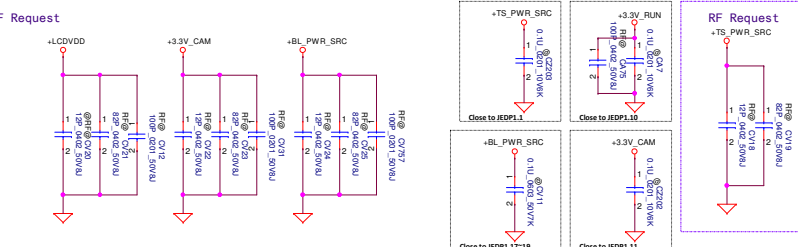
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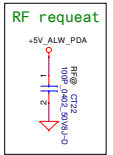
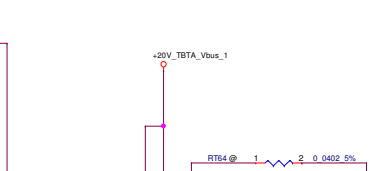
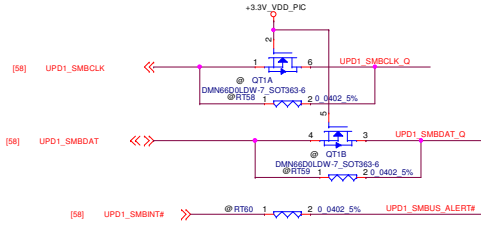


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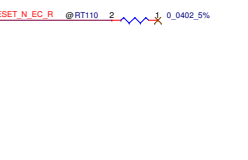
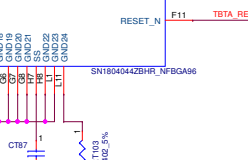
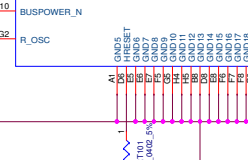
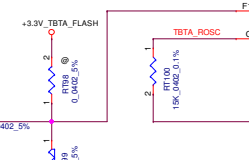
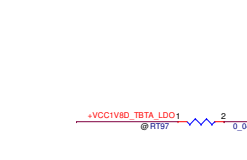
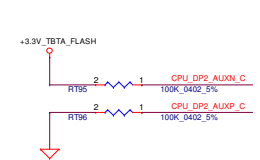
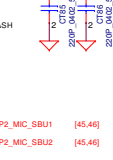
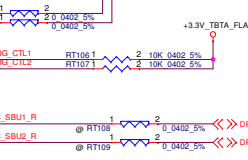
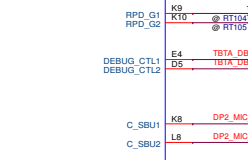
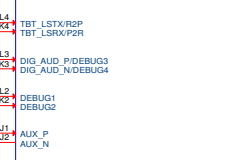
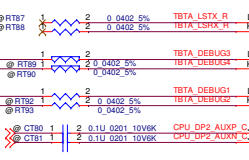
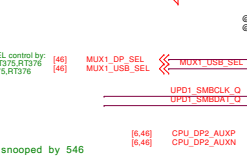
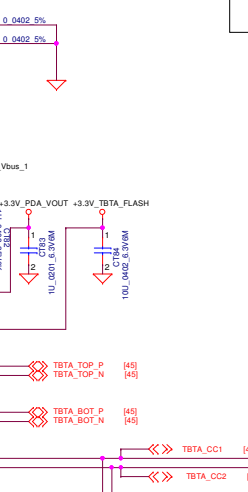
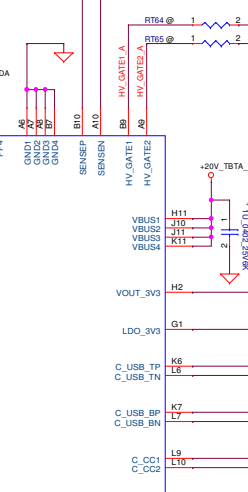
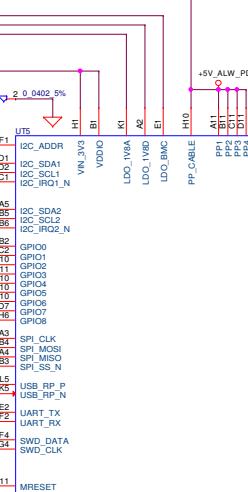
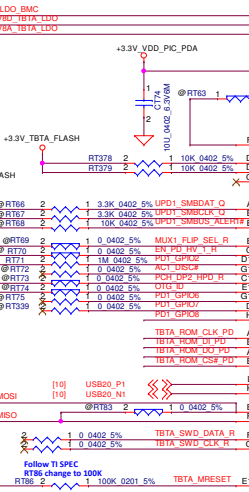
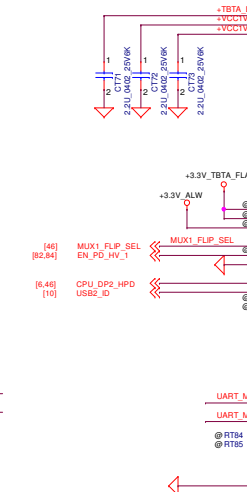
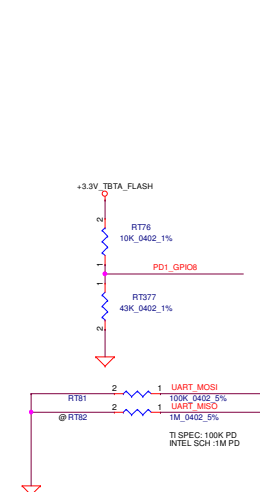
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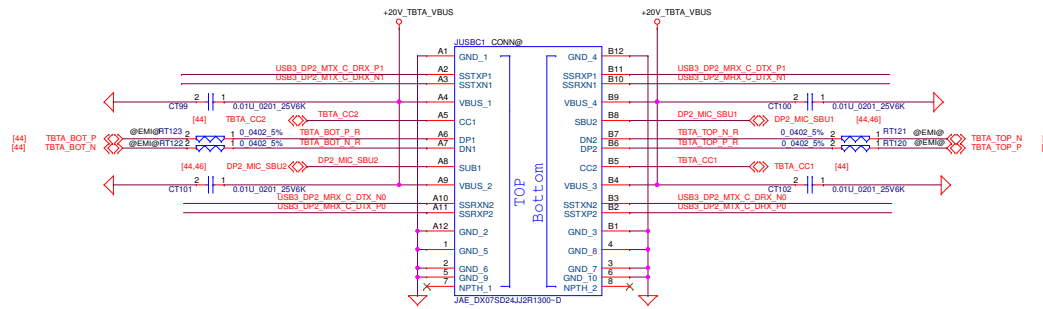
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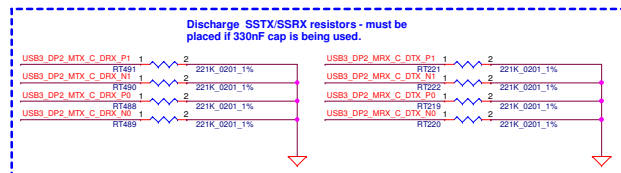
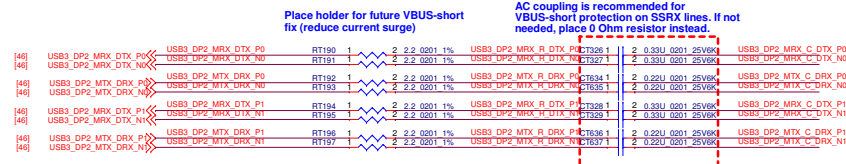
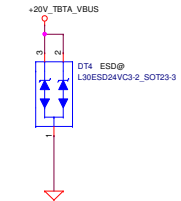
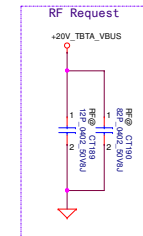
DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UPF only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TiVD supported
0.10	0.18	1	UPF only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9-3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes /Sink, C and D pin configuration TiVD supported
0.20	0.28	2	UPF only 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TiVD supported
0.30	0.38	3	UPF only 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes /Sink, C and D pin configuration TiVD supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TiVD supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes /Source, C, D, and E pin configurations. TiVD supported Accepts power role swaps but will not initiate. <u>Accepts data role swap to UFP and can initiate.</u>
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @0.9A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes /Source, C, D, and E pin configurations. TiVD supported Accepts power role swaps but will not initiate. <u>Accepts data role swap to DFP and can initiate.</u>
0.70	1.00	7	Infinite boot retry from Flash to Host and FV cycles.



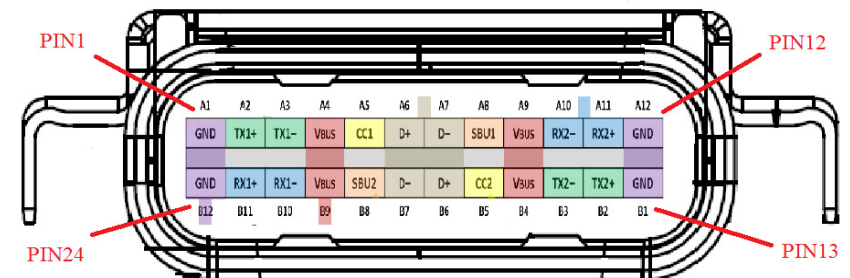
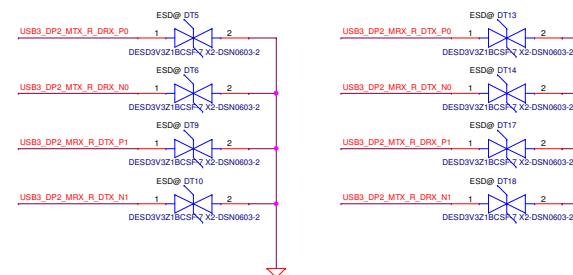
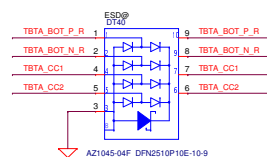
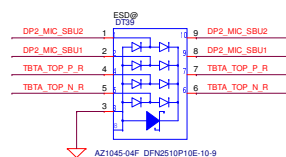
CT630-633 use SD043000080 (0 ohm) for CSLP3 build

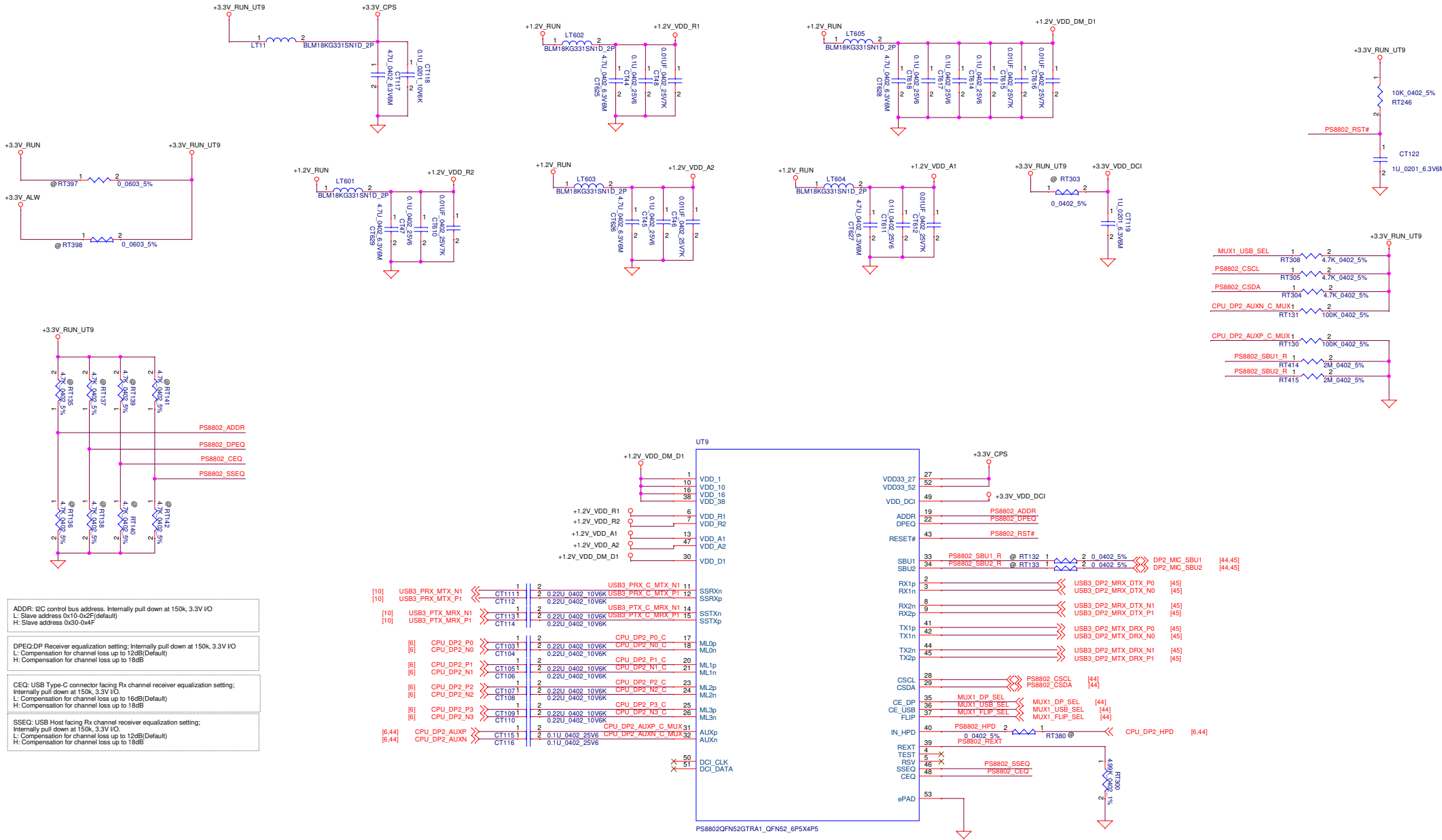


Link DX07SD24J2R1300 done 0123



change typeC ESD part from SC40000AR00 to SC40000DF00





ADDR: I2C control bus address. Internally pull down at 150k, 3.3V I/O
L: Slave address 0x10-0x0F (Default)
H: Slave address 0x30-0x4F

DPEQ: DP Receiver equalization setting. Internally pull down at 150k, 3.3V I/O
L: Compensation for channel loss up to 12dB (Default)
H: Compensation for channel loss up to 18dB

CEQ: USB Type-C connector facing Rx channel receiver equalization setting;
Internally pull down at 150k, 3.3V I/O
L: Compensation for channel loss up to 16dB (Default)
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting;
Internally pull down at 150k, 3.3V I/O
L: Compensation for channel loss up to 12dB (Default)
H: Compensation for channel loss up to 18dB

change from SA0000AIM10(A1) to SA0000AIM20(A2)

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Issued Date		Deciphered Date		Title	
2016/01/01		2017/01/01		DP/USB3 Re-timer PS8802	
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DP/USB3 Re-timer PS8802

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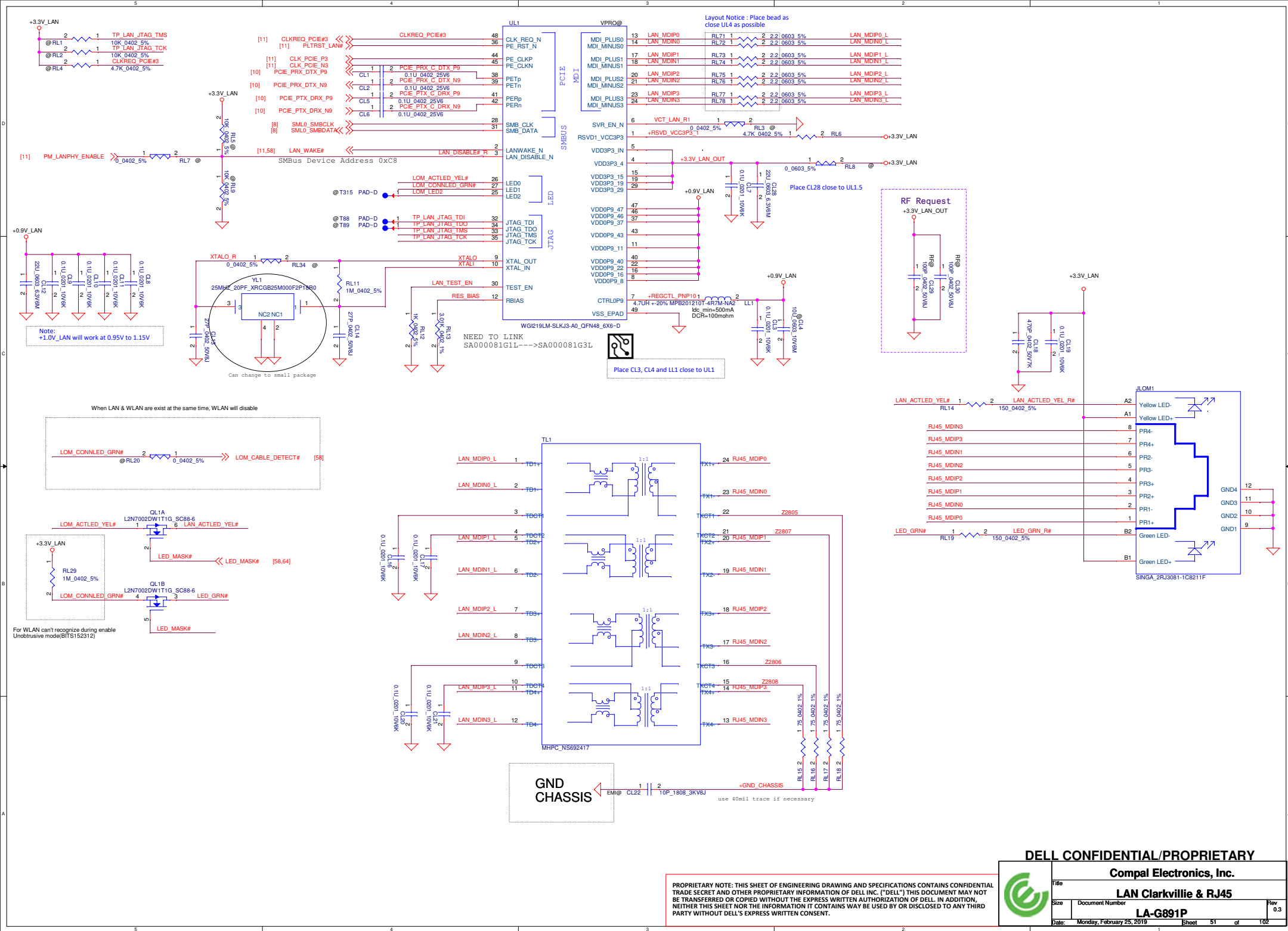
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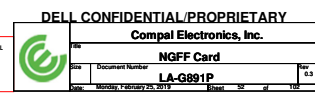
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NGFF slot E Key E



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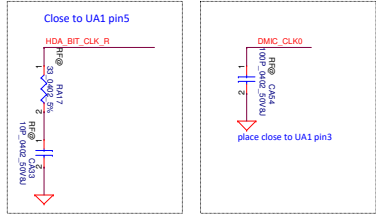
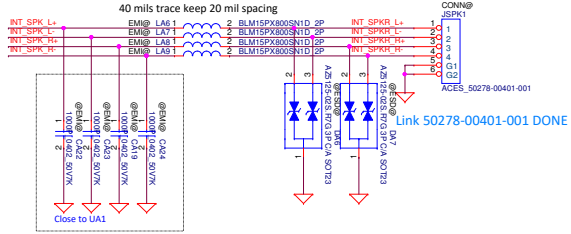
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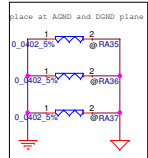
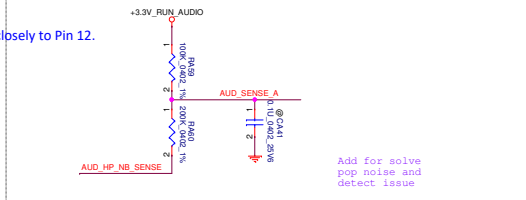
1W x 1ch, 4ohm (Transducer spec is 80hm/0.5Watt per unit, there are two transducer units in one speaker box)

Internal Speakers Header

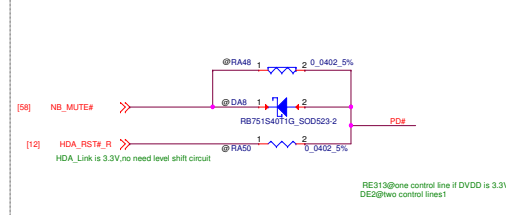
40 mils trace keep 20 mil spacing



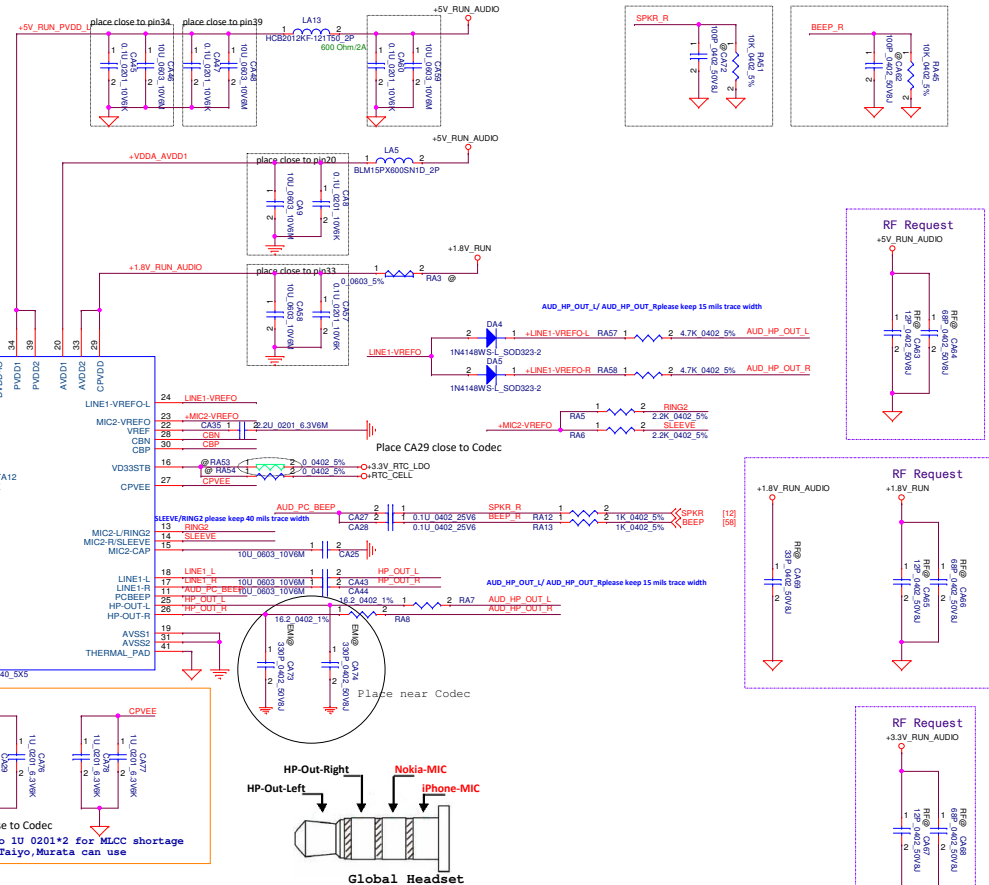
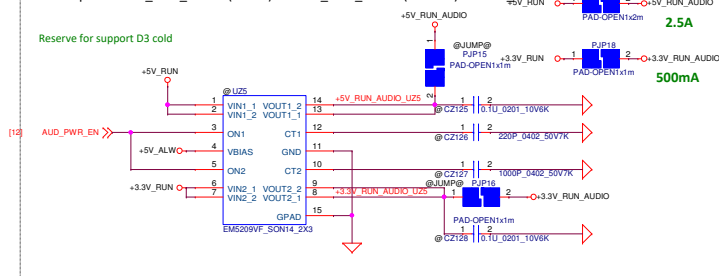
Place closely to Pin 12.



CLASS-D POWER DOWN CONTROL CIRCUIT

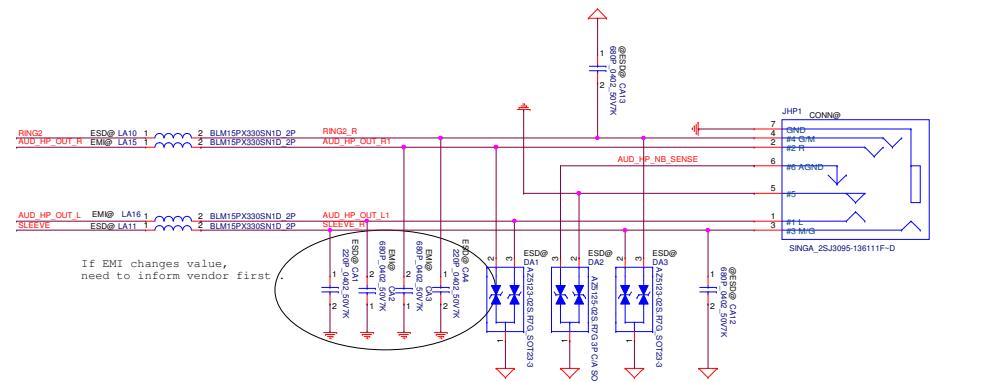


Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN



Universal Jack

Add this Filter to avoid other components/chips be influenced



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Codec ALC3204

LA-G891P

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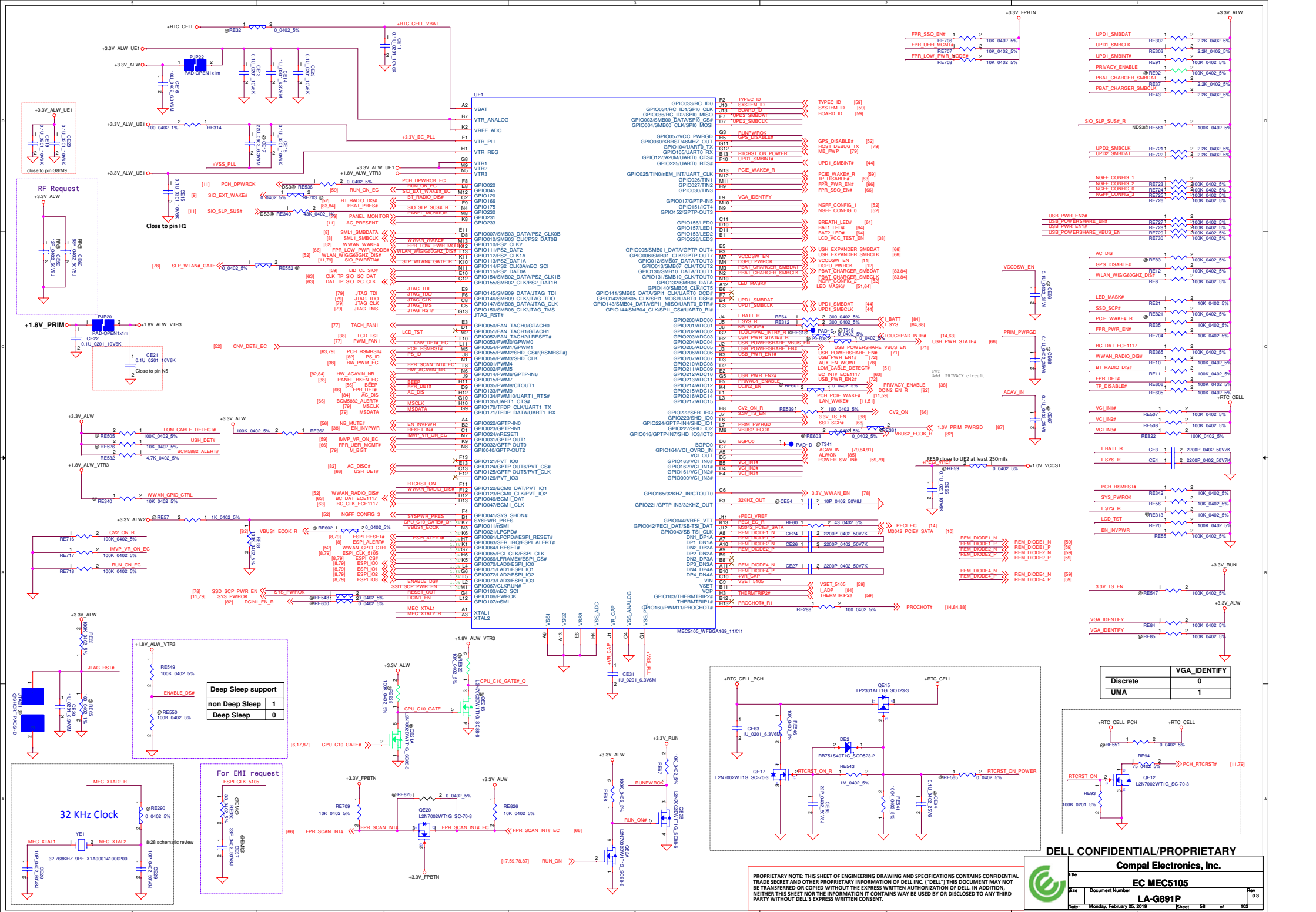
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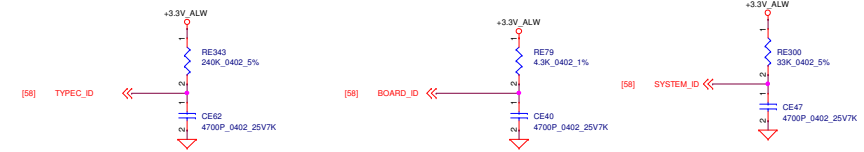
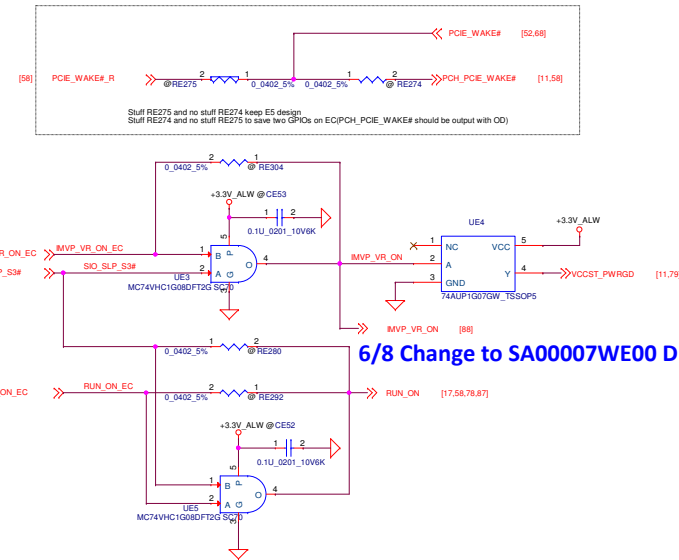
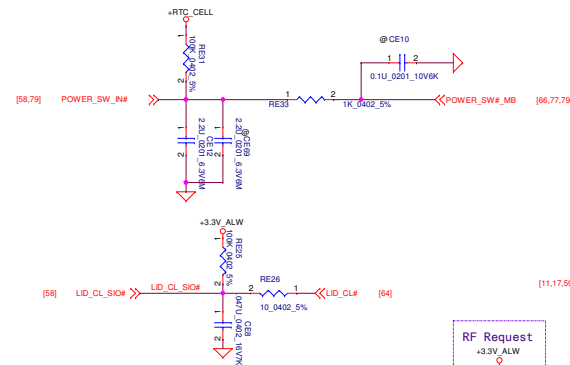
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Compal Electronics, Inc.			
Title			
Audio Amplifier			
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	RE343	CE62	REV
*	240K	4700p	Single Port ACE w/o AR
	130K	4700p	Single Port ACE w/AR
	62K	4700p	Dual Port ACE w/o AR
	33K	4700p	Dual Port ACE w/AR
	8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
	4.3K	4700p	
	2K	4700p	
	1K	4700p	

RE79	CE40	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	reserved
* 4.3K	4700p	A00
2K	4700p	
1K	4700p	

	RE300	CE47	PANEL SIZE
	240K	4700p	11"
	130K	4700p	12"
	62K	4700p	13"
*	33K	4700p	14"
	8.2K	4700p	15"
	4.3K	4700p	17"
	2K	4700p	15P
	1K	4700p	

PD_ACE_DET# rise time is measured from 5%~68%.

BOARD_ID rise time is measured from 5%~68%.

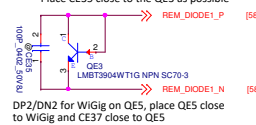
SYSTEM_ID rise time is measured from 5%~68%.



Thermal diode mapping

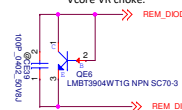
5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	M.2
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place CE35 close to the QE3 as possible

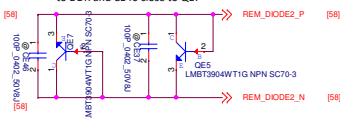


DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.



DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

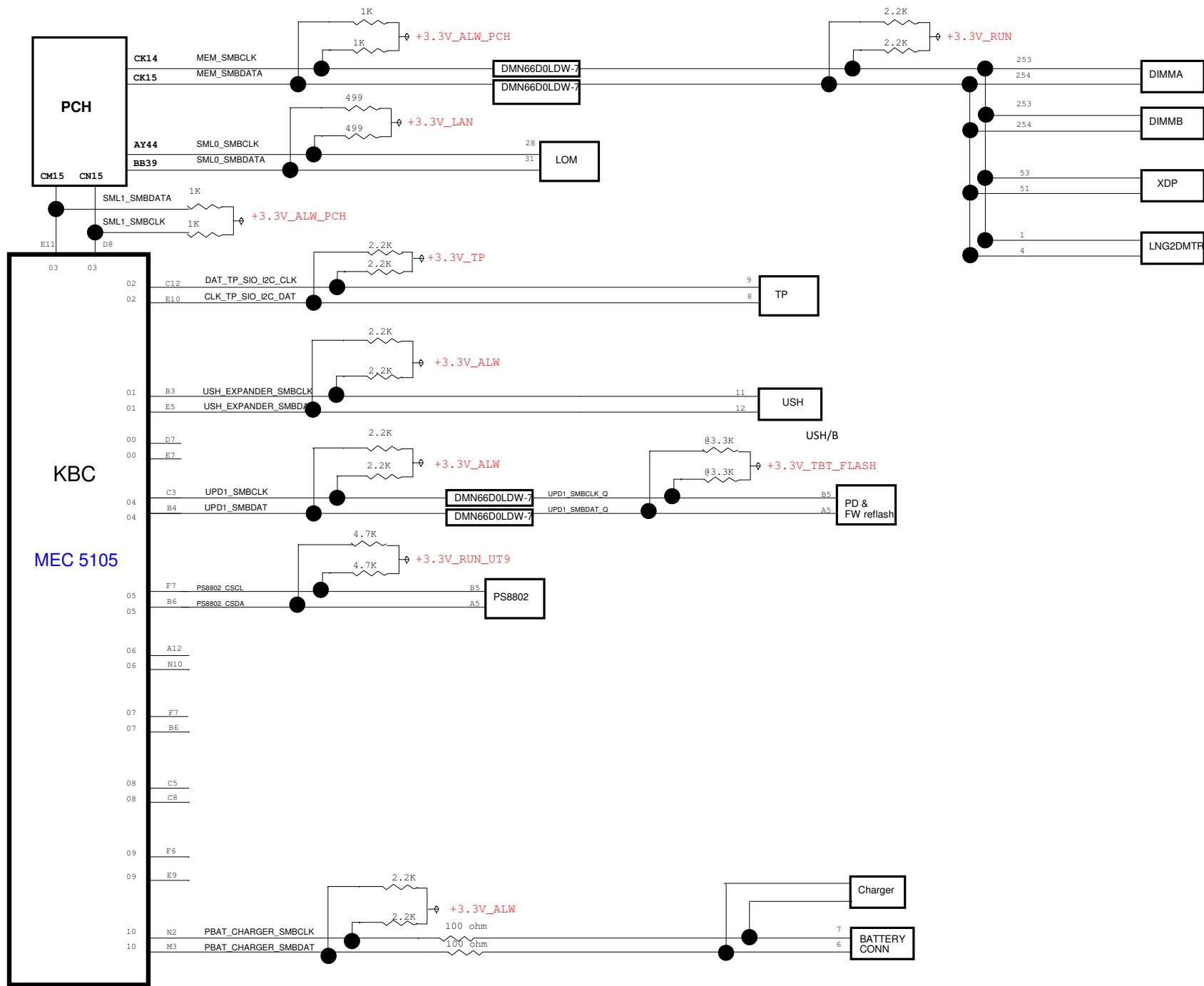


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Compal Electronics, Inc.			
Title		Secure & Reset IC	
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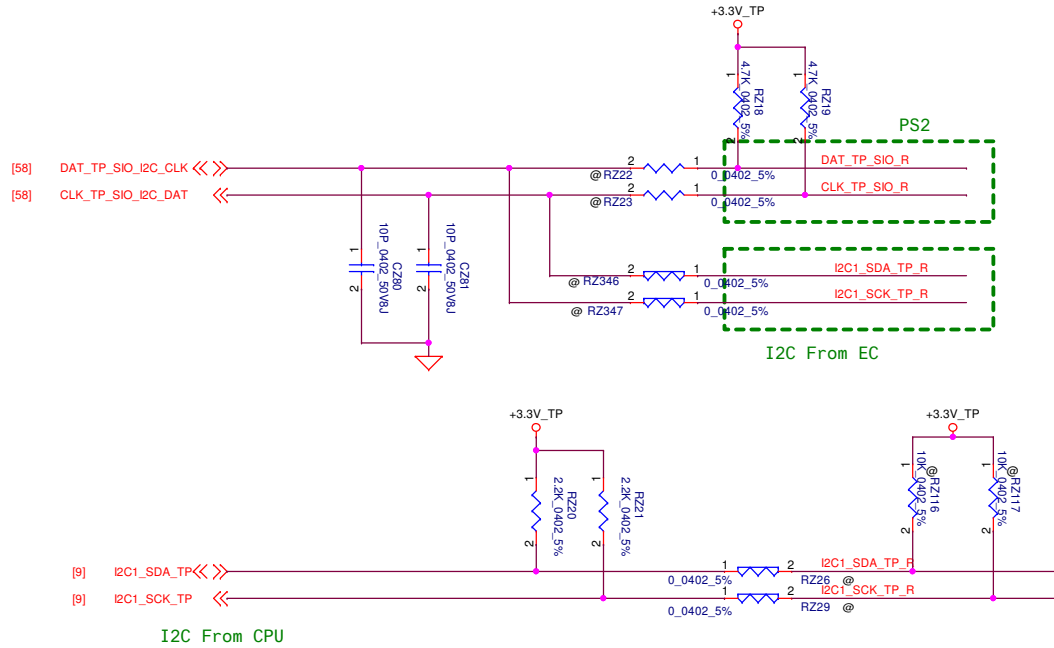
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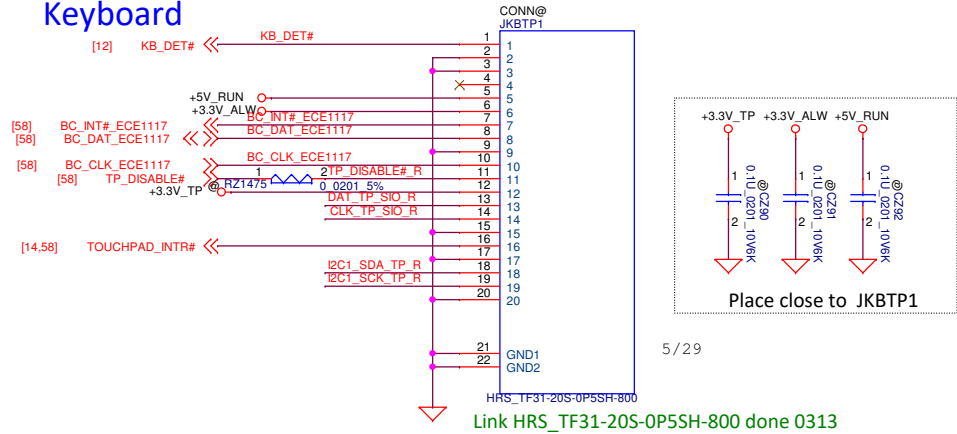
DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title	LED (Controller)		
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Touch Pad

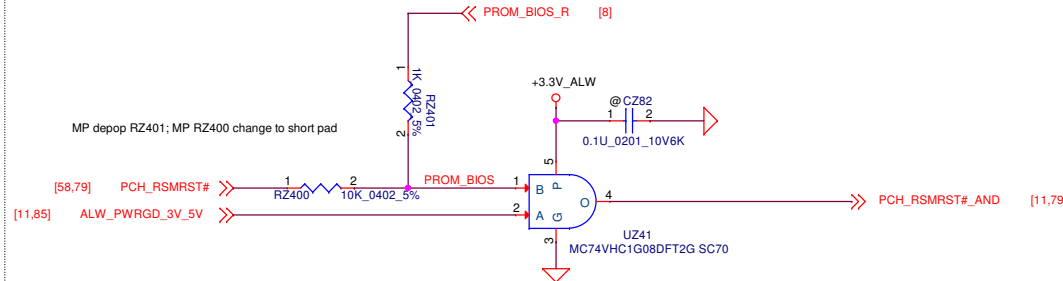


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

Keyboard



RSMRST circuit



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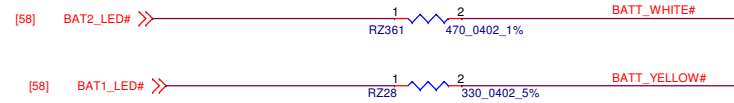
Compal Electronics, Inc.

Keyboard

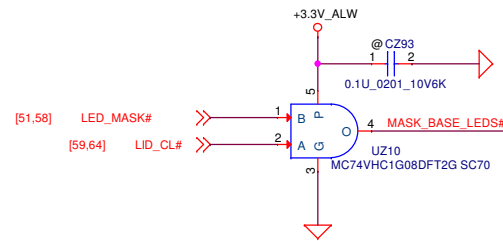
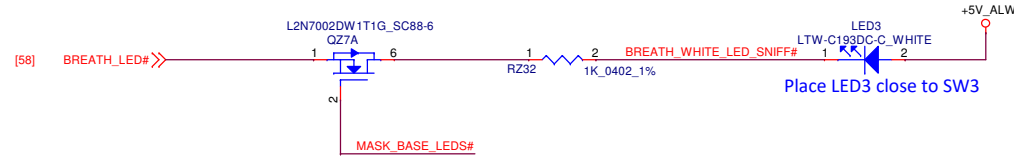
LA-G891P

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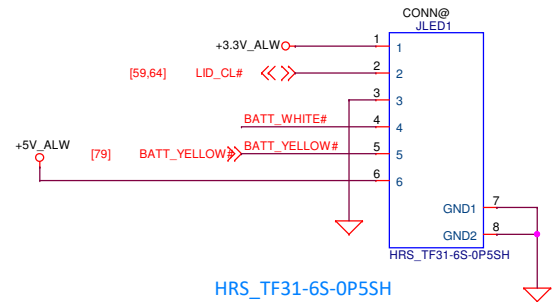
Battery LED



Breath LED



LED board CONN



LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

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Title	LED & LID	Rev	0.3
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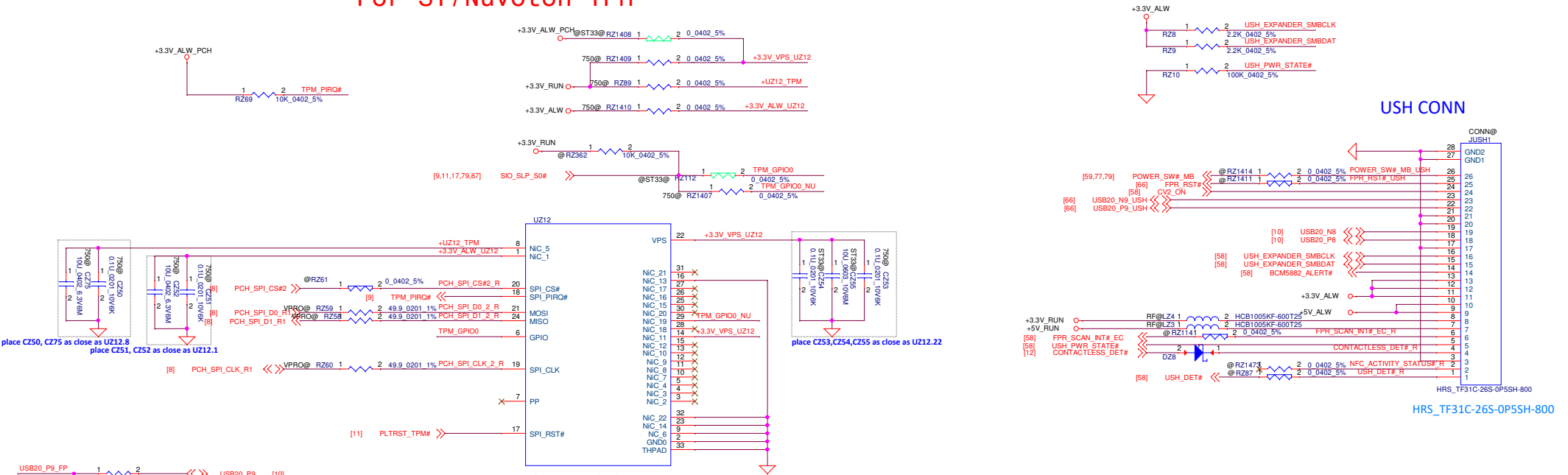
Reserve

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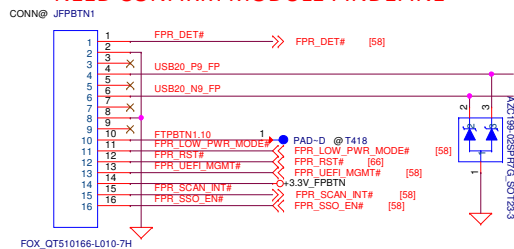


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Compal Electronics, Inc.			
Title	KB/TP/LED/LID		
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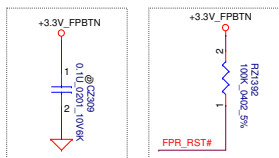
For ST/Nuvoton TPM



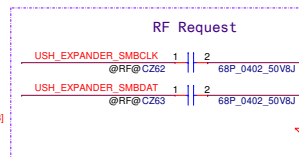
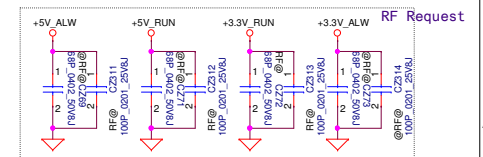
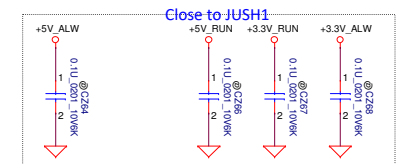
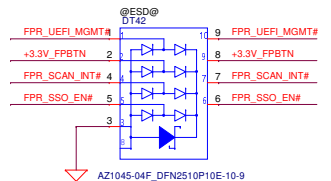
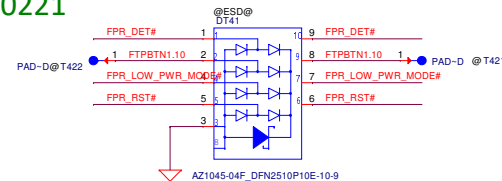
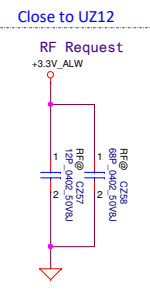
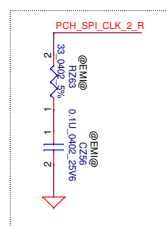
FP in PWR BUTTON connector
NEED CONFIRM MODULE PINDEFINE



Link FOX_QT510166-L010-7H done



Compal MB CONN Symbol	Signal	FPR Symbol
2	GND	1
4	USB DP(D+)	2
6	USB DM(D-)	3
8	GND	4
10	RESERVED	5
12	FP RESET#	6
14	+3.3V_FPBTN	7
16	FPR_S5O_EN#	8
15	FPR_SCAN_INT#	9
13	FPR_UEFI_MGMT#	10
11	FPR_LOW_PWR_MODE#	11
9	NA	12
7	NA	13
5	NA	14
3	NA	15
1	FPR_DET(GND)	16



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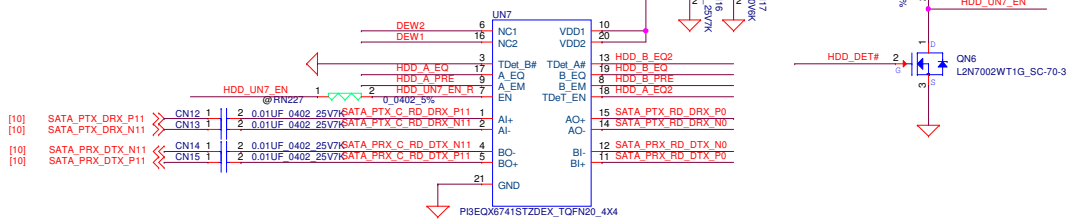
Compal Electronics, Inc.



Title			
MEC5105 support			
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	pin 3	pin 6	pin 13	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDet_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

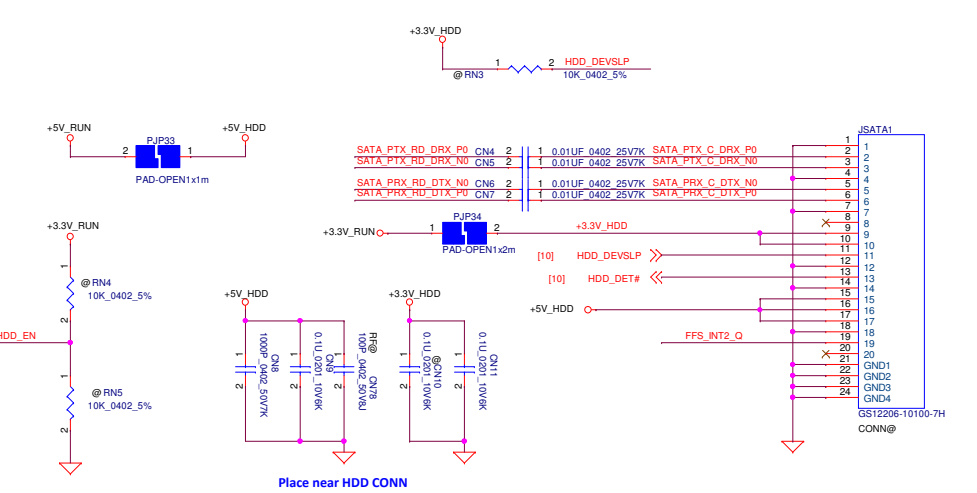
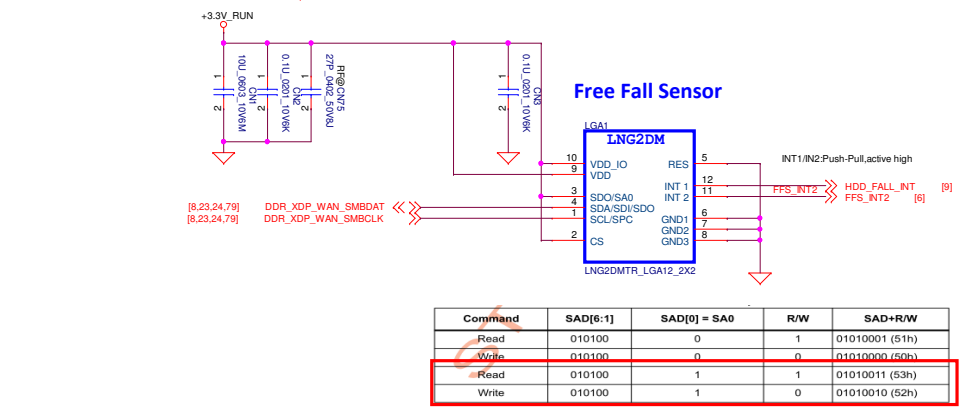
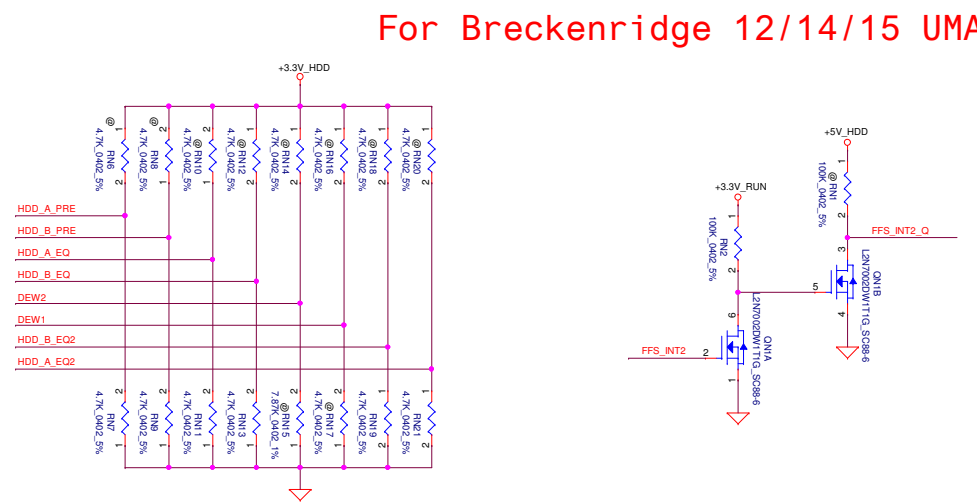
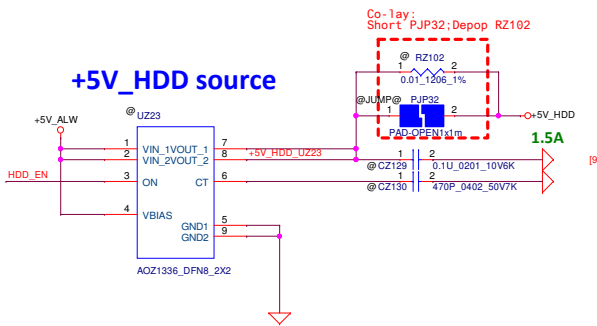
SATA Repeater



	HDD_A_EQ	HDD_B_EQ	HDD_A_EQ2	HDD_B_EQ2	DEW1	DEW2	HDD_A_PRE	HDD_B_PRE
Pericom PI3EQX6741ST	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
TI SN75LVCP601	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (IPU)	NC (IPU)	PH (RN6)	PH (RN8)
Parade PS8527C	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC (1/2 VDD)	NC (1/2 VDD)

*				A_EQ	B_EQ		A_EM	B_EM	
	Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB	
	2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB	
	3rd	Parade	EQ2	EQ1	A_EQ	B_EQ		A_EM	B_EM
			(M = VDD/2)						
			0	M	2.4dB	2.4dB	0 M 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB
			0	0	7.4dB	7.4dB			
			0	1	14.4dB	14.4dB			
			M	M	12.2dB	12.2dB			
			M	0	9.4dB	9.4dB			
			M	1	13.3dB	13.3dB			
			1	M	6.2dB	6.2dB			
1	0	11.2dB	11.2dB						
1	1	5dB	5dB						

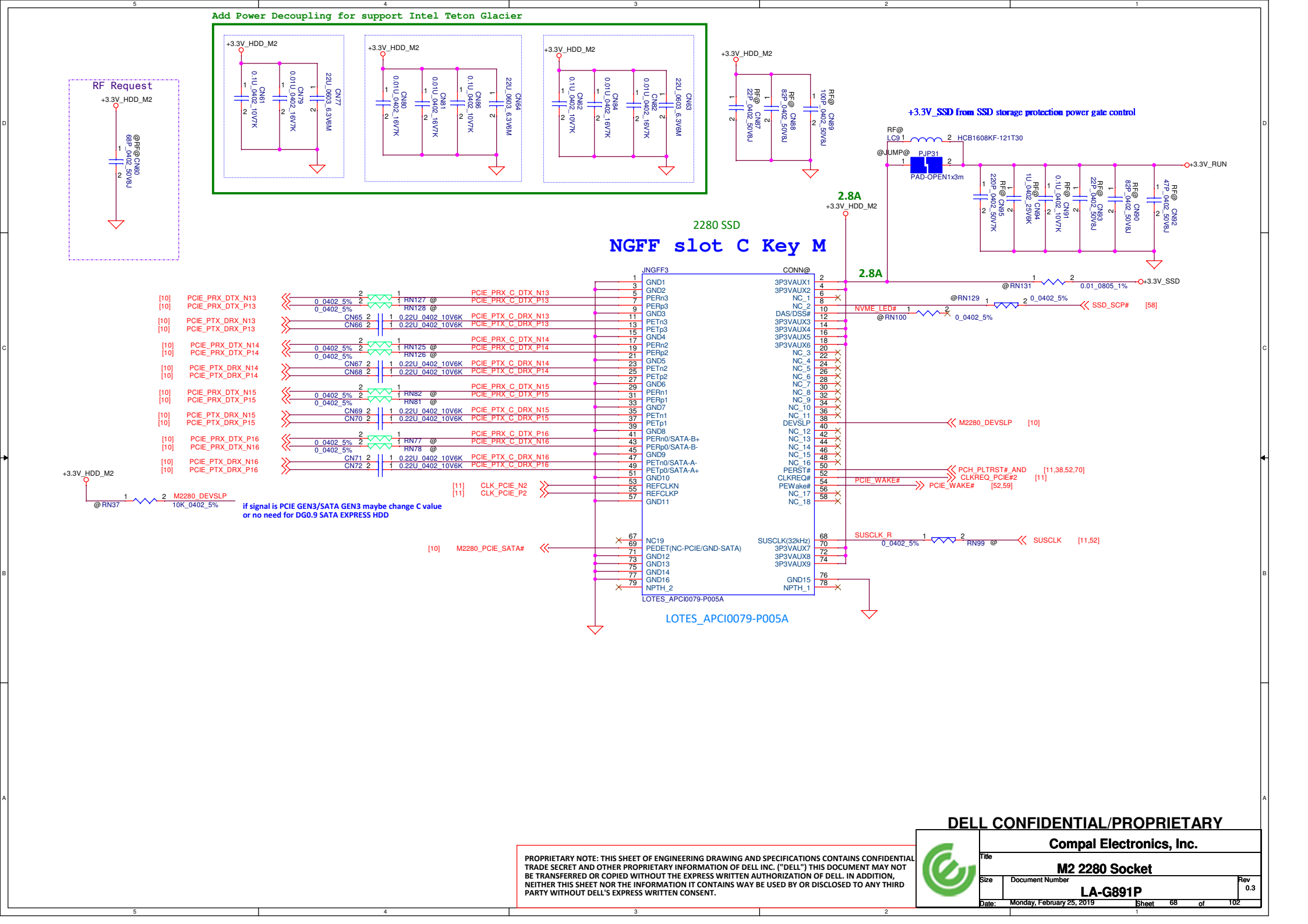
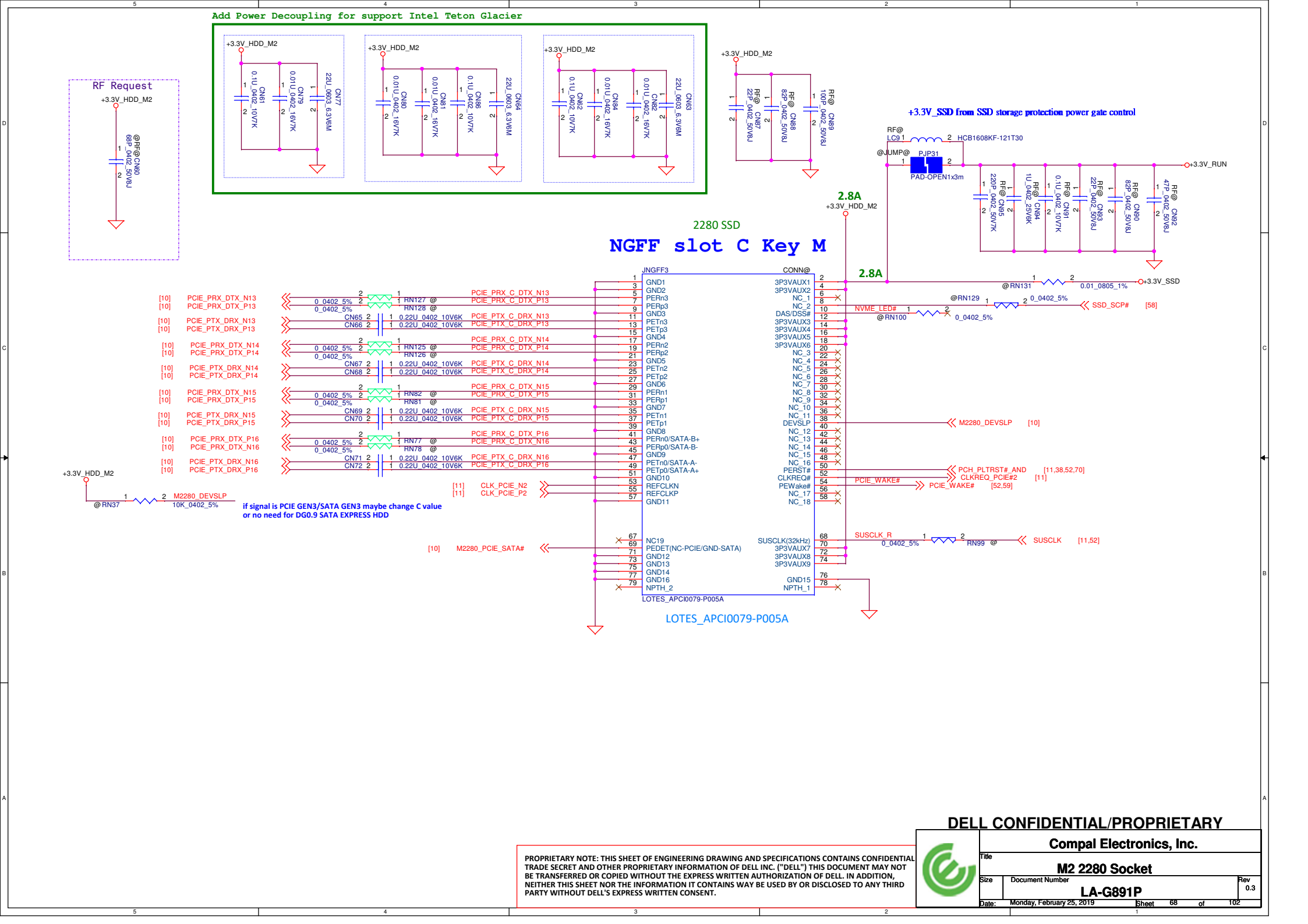
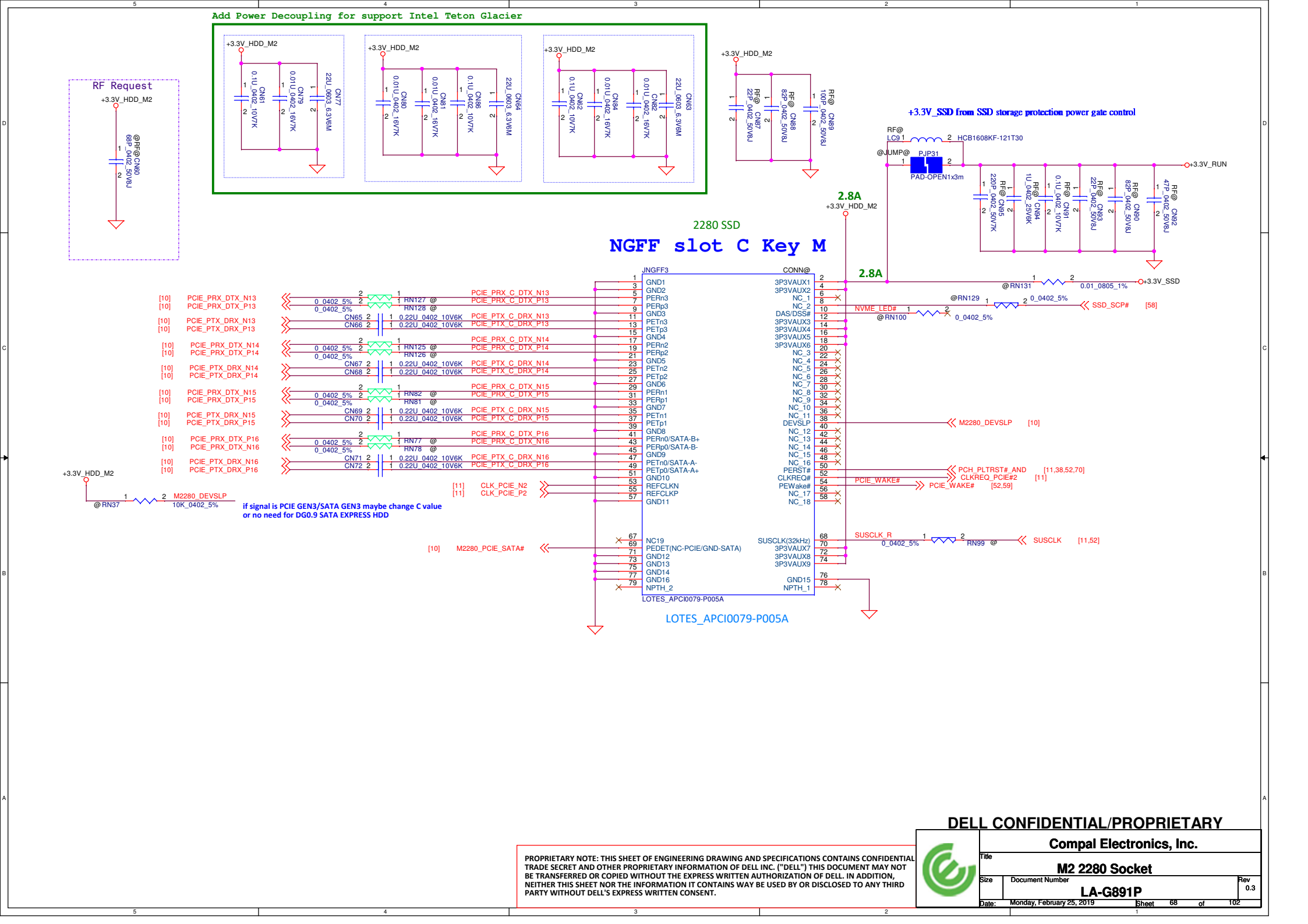
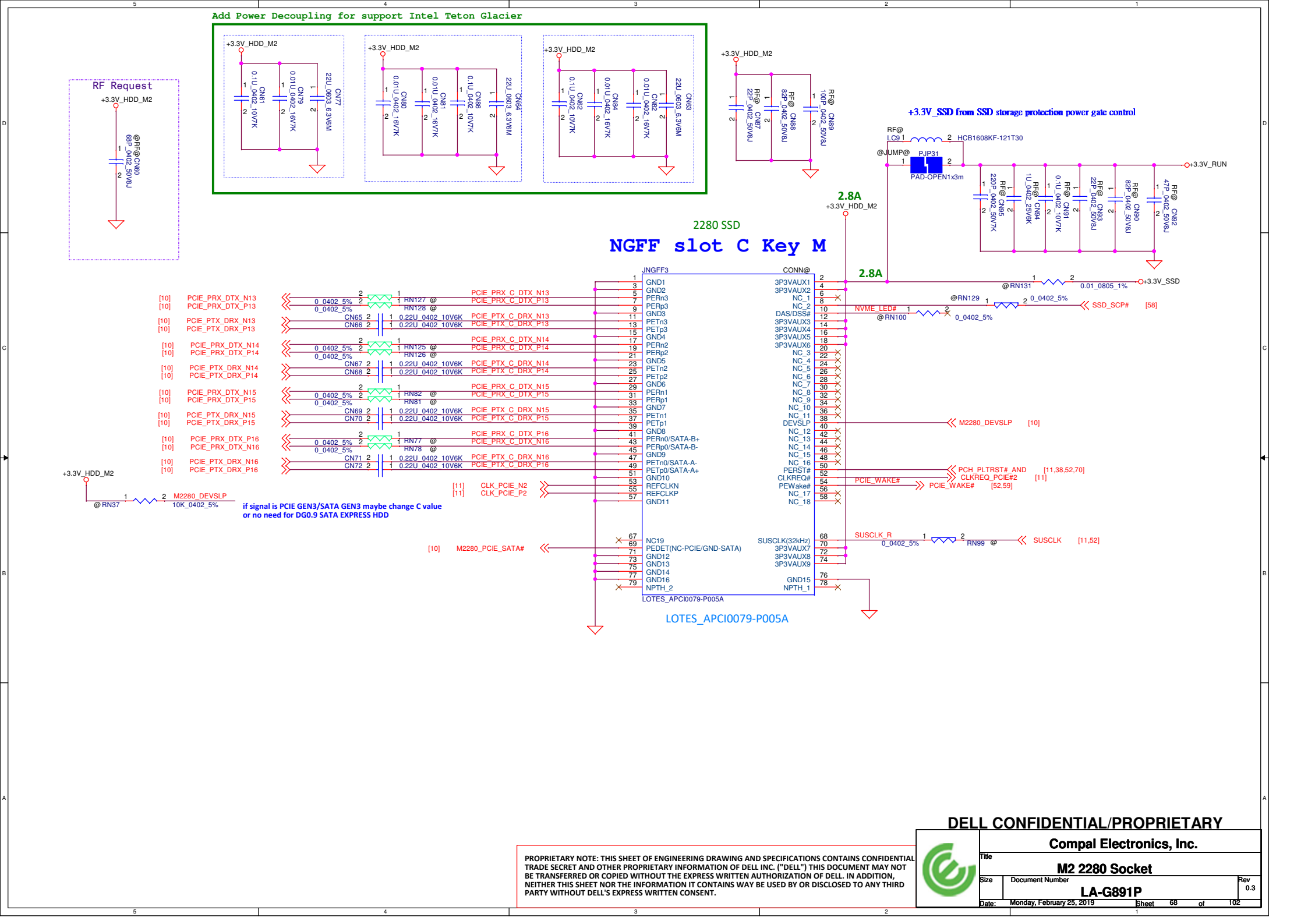
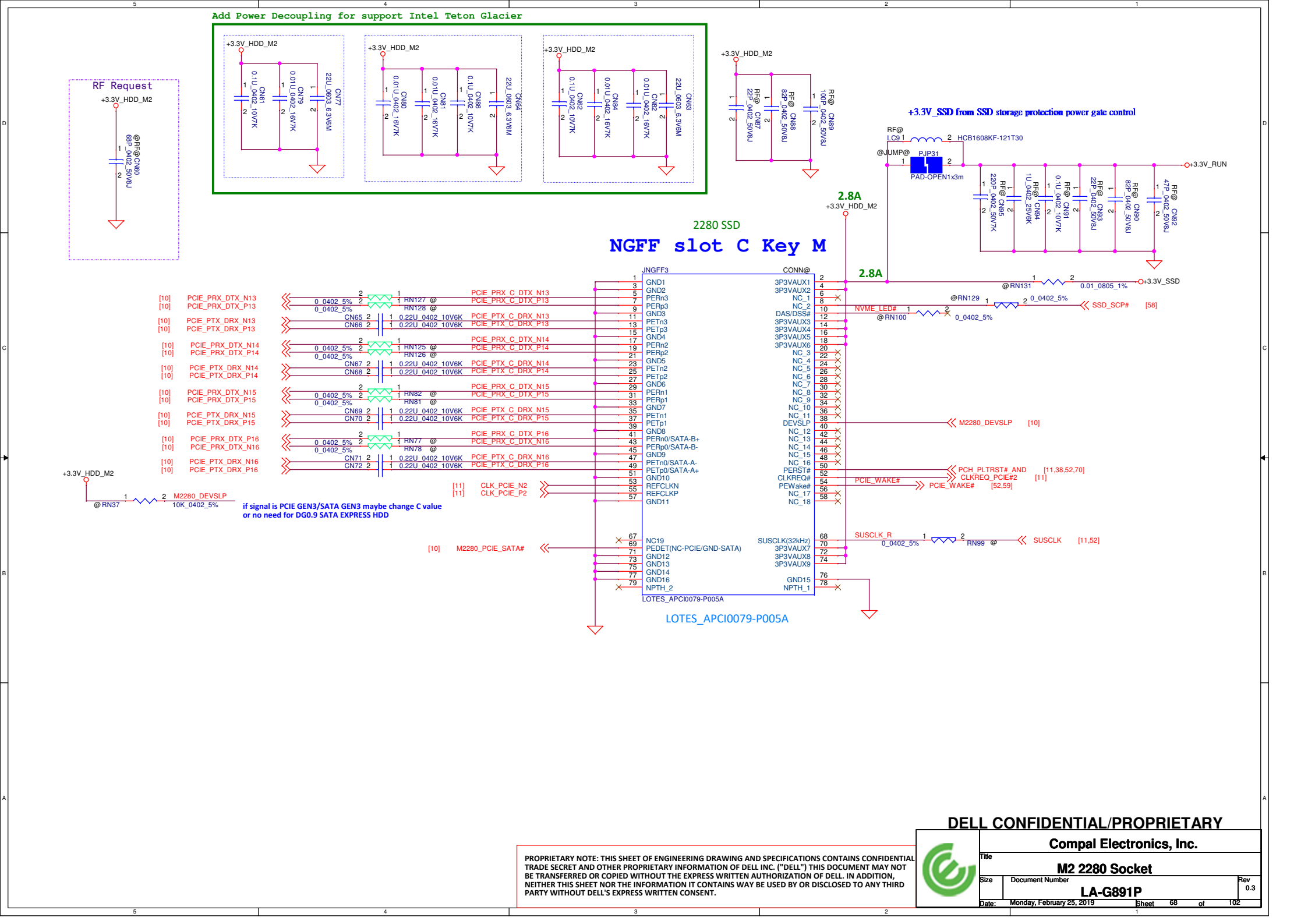
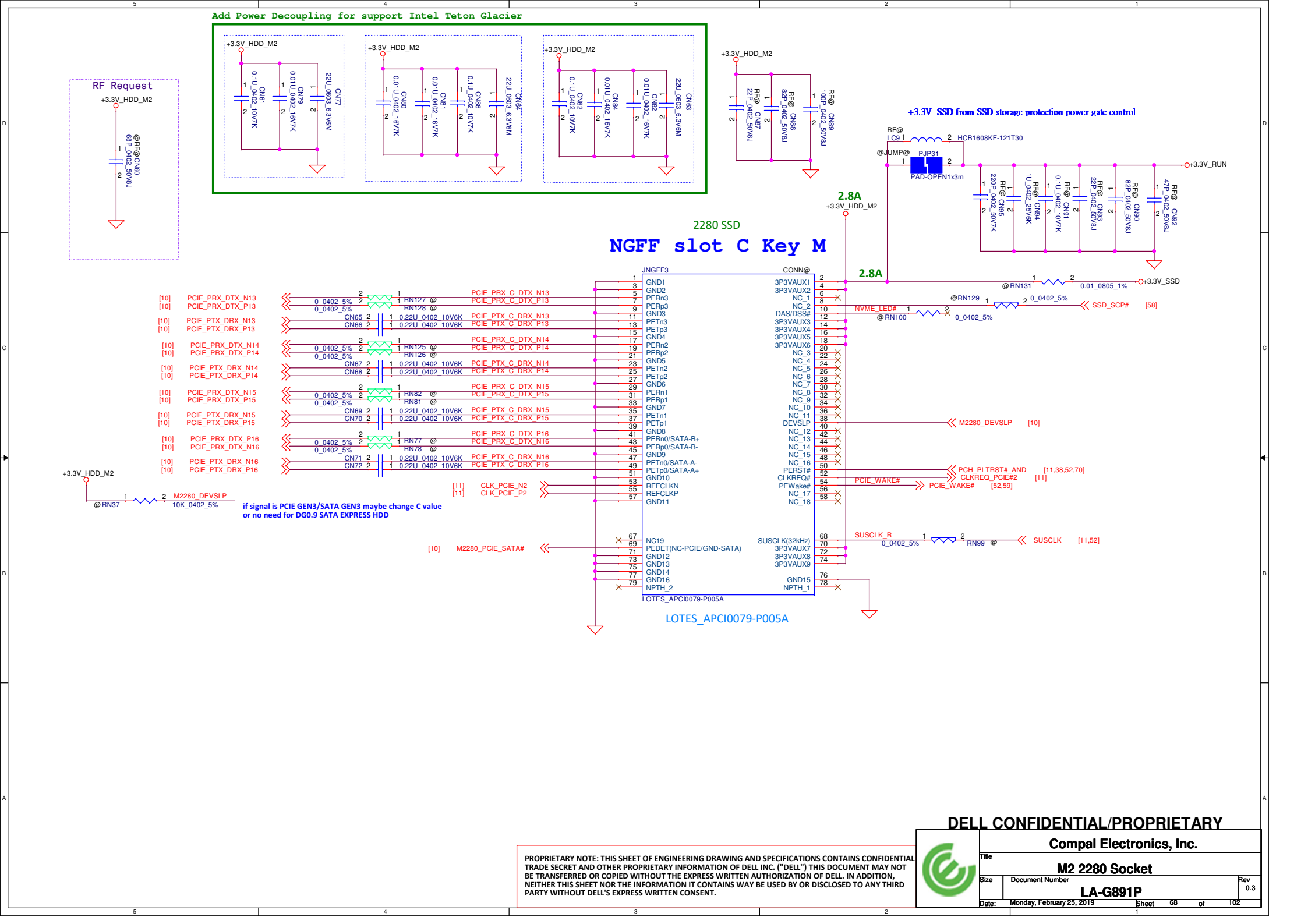
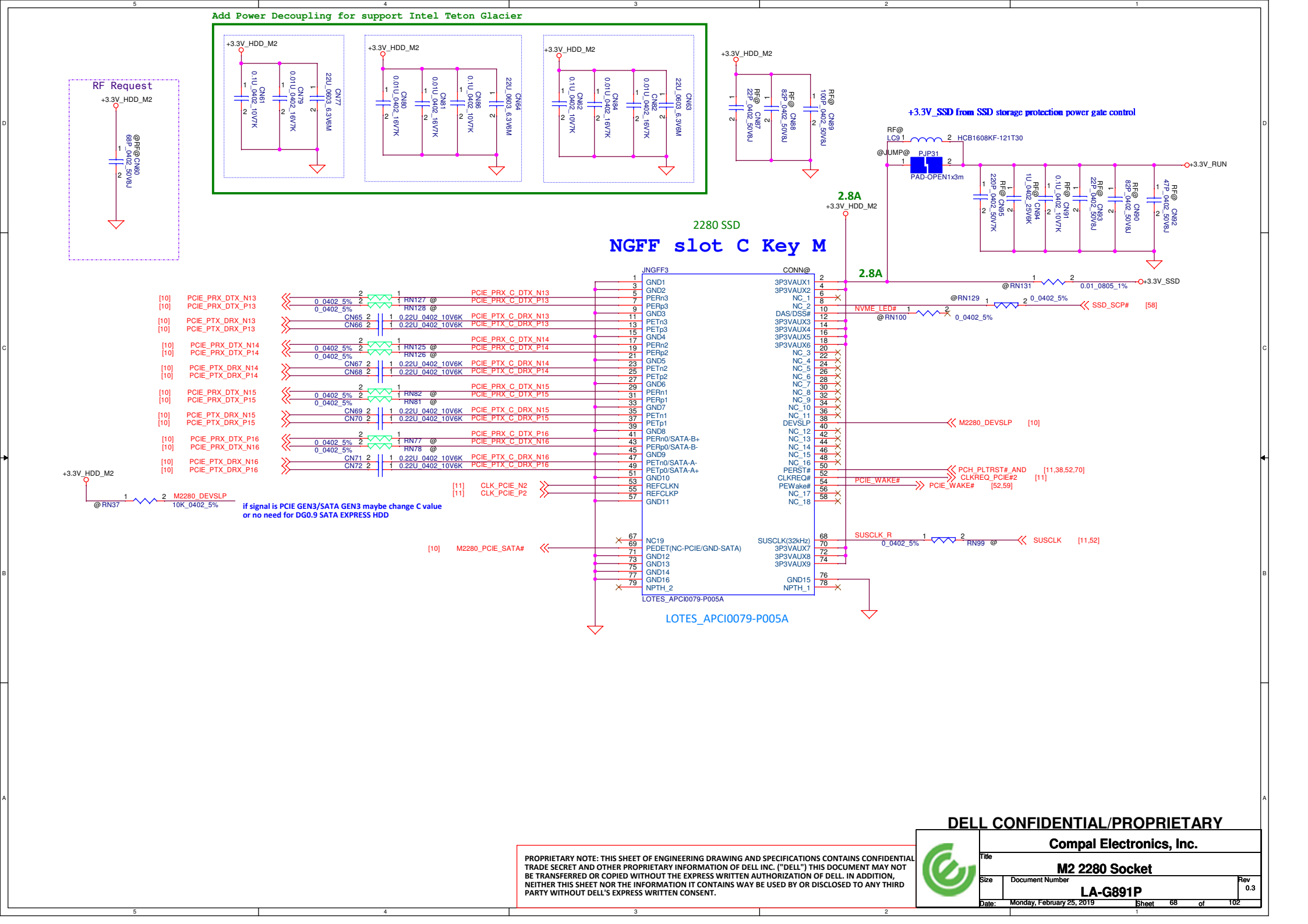
* red color is current setting



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Compal Electronics, Inc.			
SATA Repeater&HDD CONN			
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[illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible]

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Compal Electronics, Inc.

Title		eMMC/UFS	
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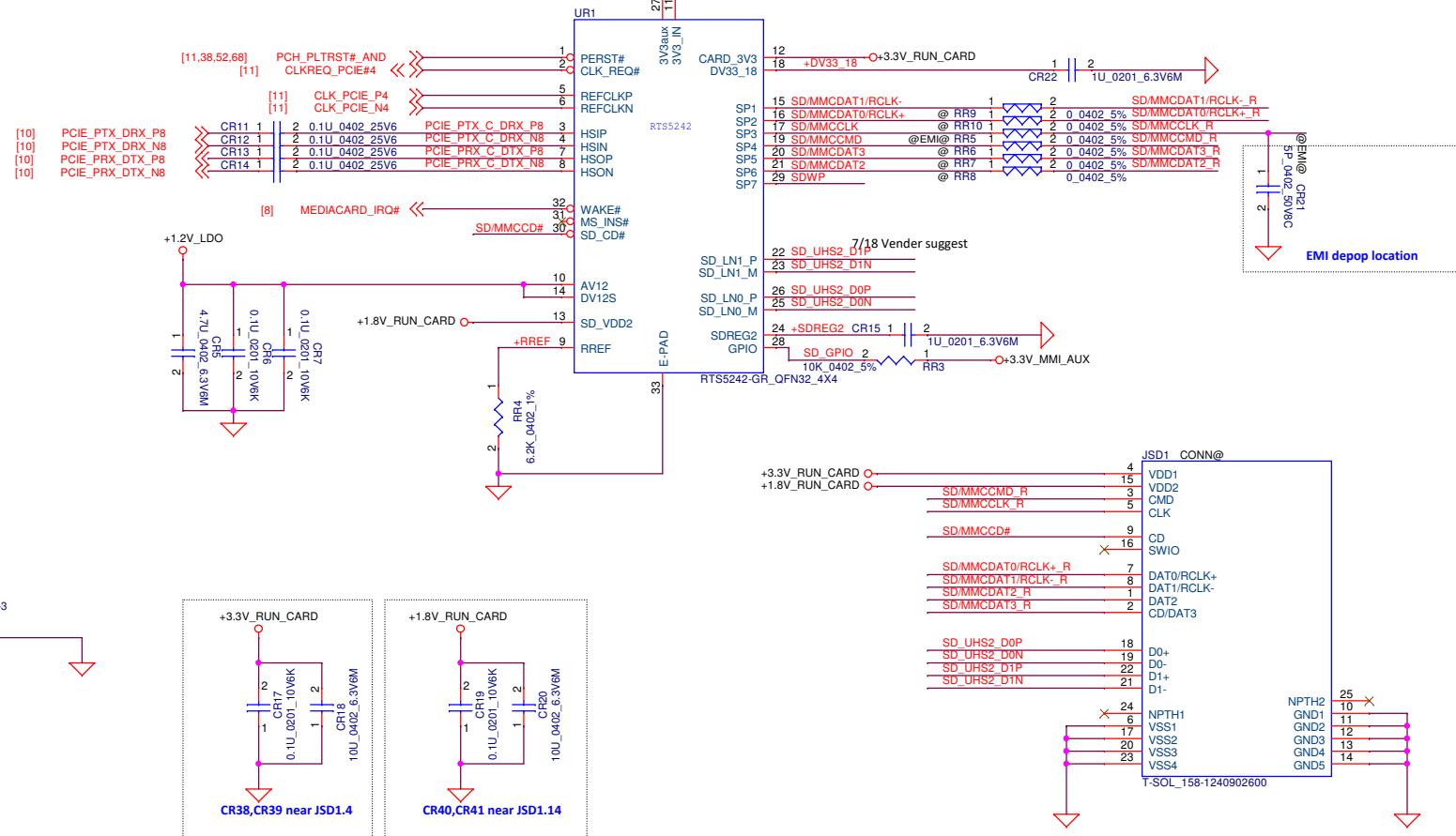
Card Reader RTS5242

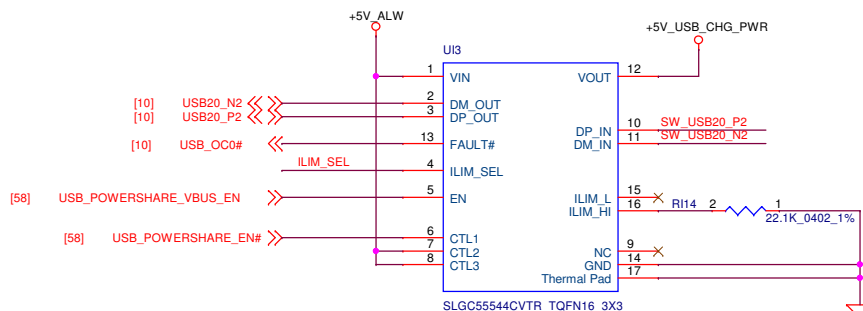
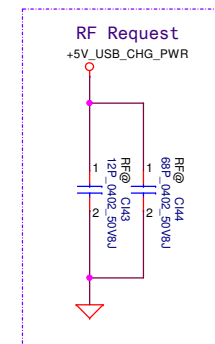
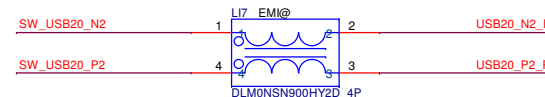
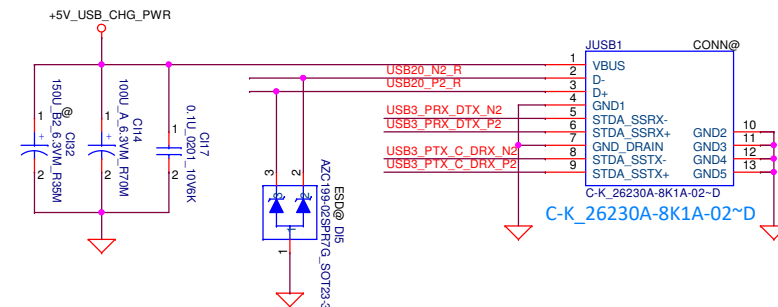
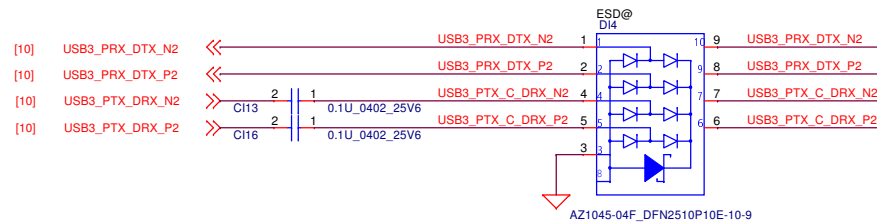
Card Reader RTS5242

LA-G891P

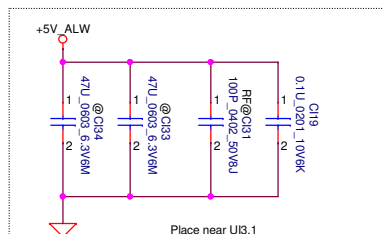
Size	Document Number	Rev
	LA-G891P	0.3
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Link Seligro SA000097E10 Done
MAIN : SLGC55544CVTR



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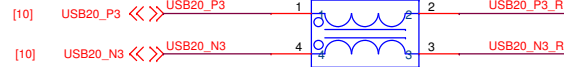
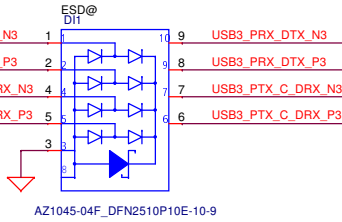
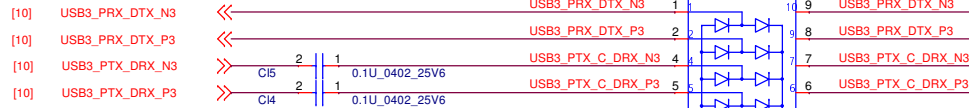
Compal Electronics, Inc.

Title		JUSB1+PS
Size	Document Number	LA-G891P
Date:	Monday, February 25, 2019	Sheet 71 of 102

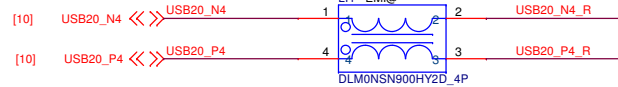
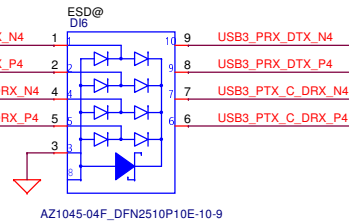
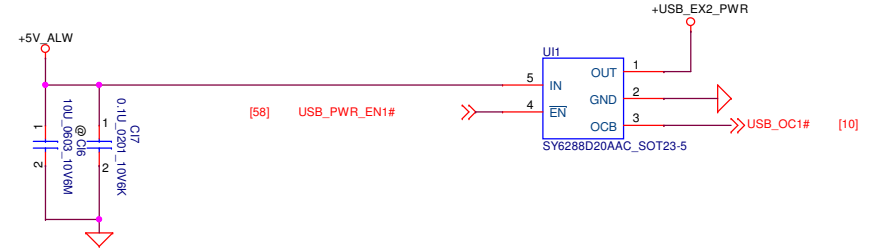
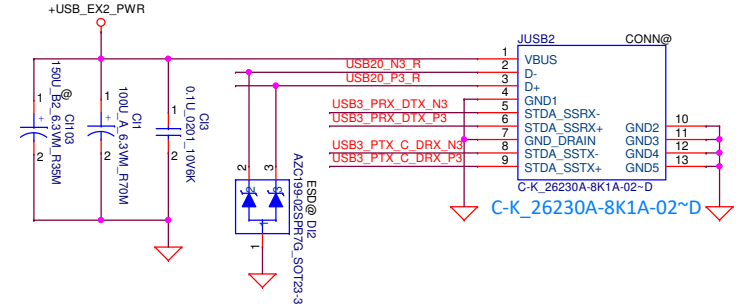
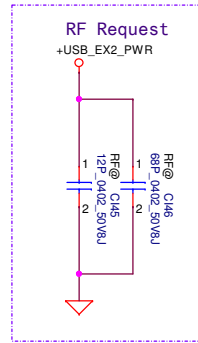
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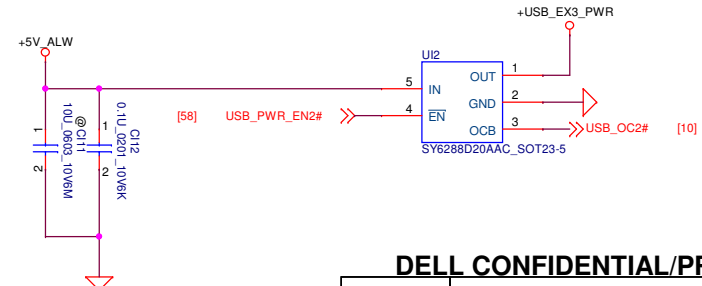
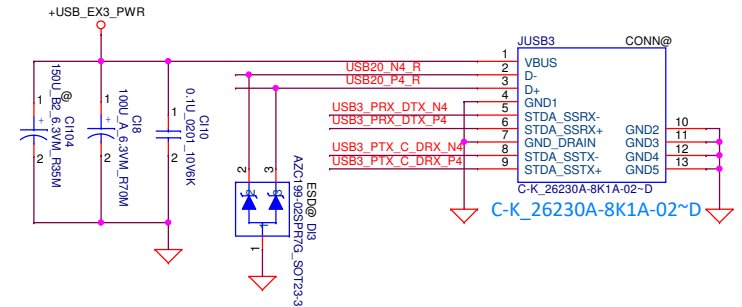
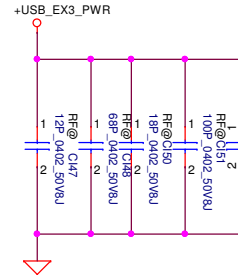
Rev 0.3



DFB request:
main SM070003Z00 (INPAO_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm



RF Request



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Compal Electronics, Inc.

Title: **JUSB2&JUSB3**

Size: Document Number

Date: Monday, February 25, 2019

Rev: 0.3

LA-G891P

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Reserve

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Compal Electronics, Inc.



Title		USB2/USB3 DB	
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Compal Electronics, Inc.			
Title		Dock	
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Reserve

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Compal Electronics, Inc.



Title		USB	
Size	Document Number		Rev
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Reserve

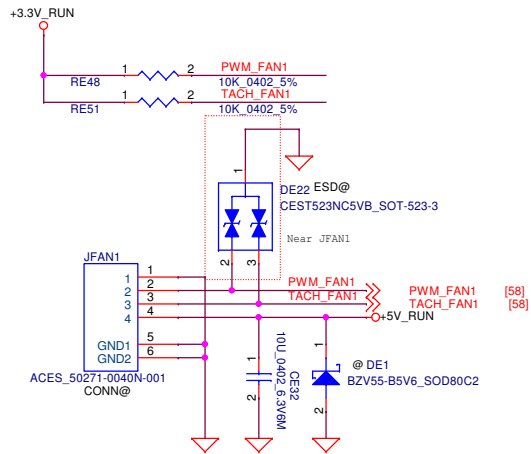
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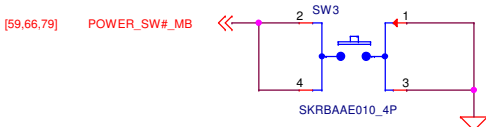
Title		USB	
Size	Document Number	LA-G891P	Rev 0.3
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Link 50271-0040N-001 DONE

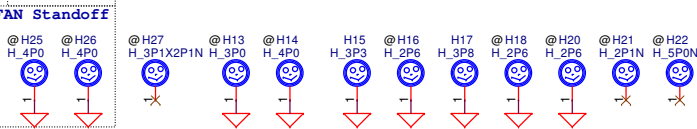
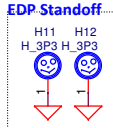
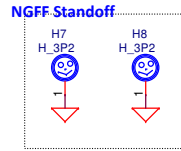
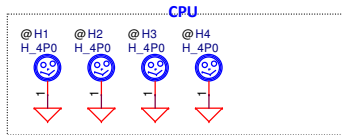
JFAN1 fan follow X9 project PIN DEFINE

POWER & INSTANT ON SWITCH TOP



Fiducial Mark

- @FD1
FIDUCIAL MARK-D
- @FD2
FIDUCIAL MARK-D
- @FD3
FIDUCIAL MARK-D
- @FD4
FIDUCIAL MARK-D



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PAD, LED

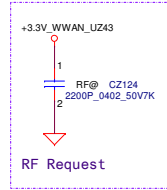
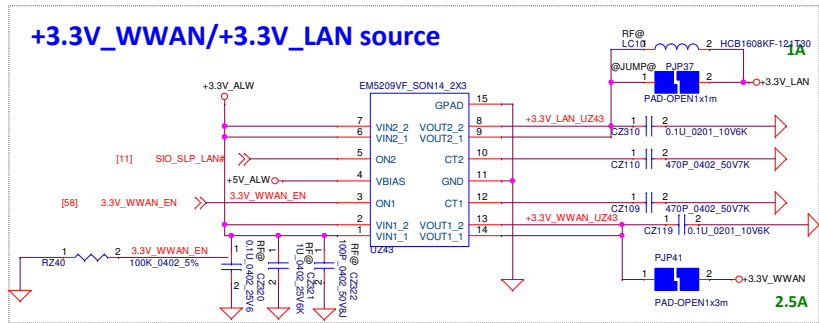
LA-G891P

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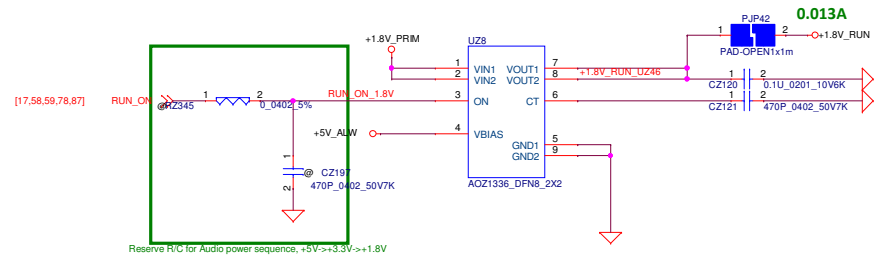


Title		PAD, LED	
Size	Document Number	Rev 0.3	
Date:	Monday, February 25, 2019	Sheet	77 of 102

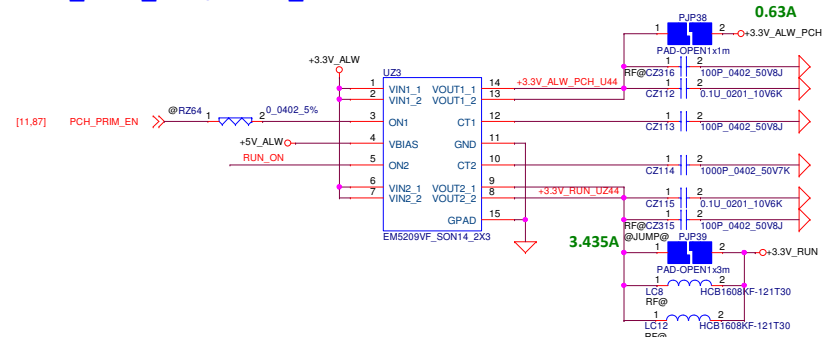
+3.3V_WWAN/+3.3V_LAN source



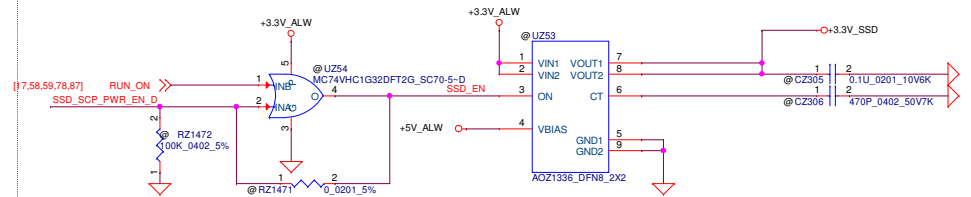
+1.8V_RUN source



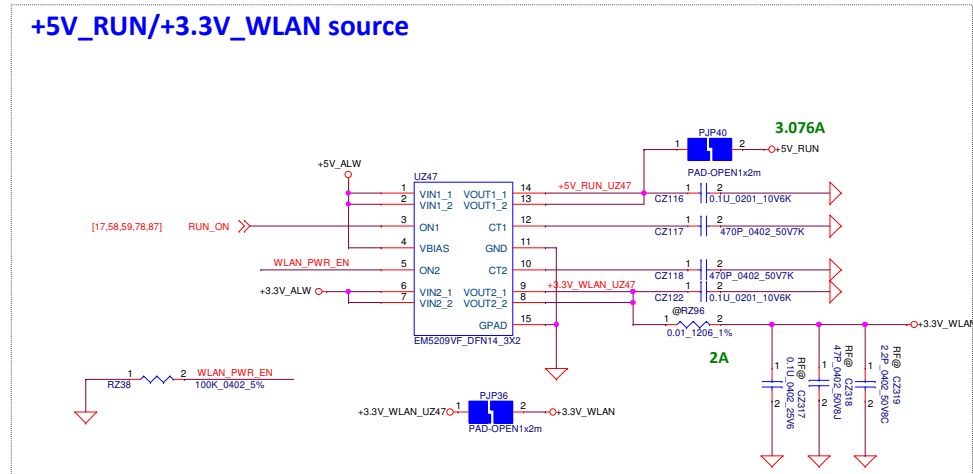
+3.3V_ALW_PCH/+3.3V_RUN source



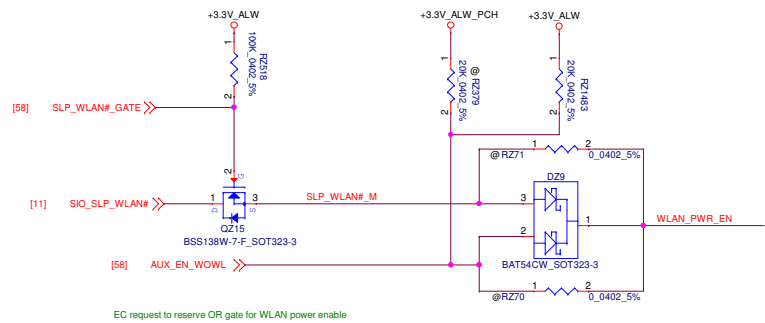
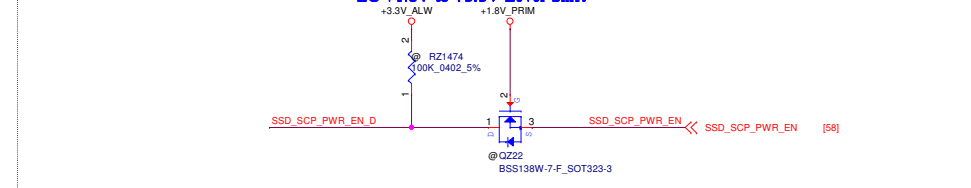
Reserve for SSD storage protection power gate control



+5V_RUN/+3.3V_WLAN source



EC +1.8V to +3.3V Level Shift



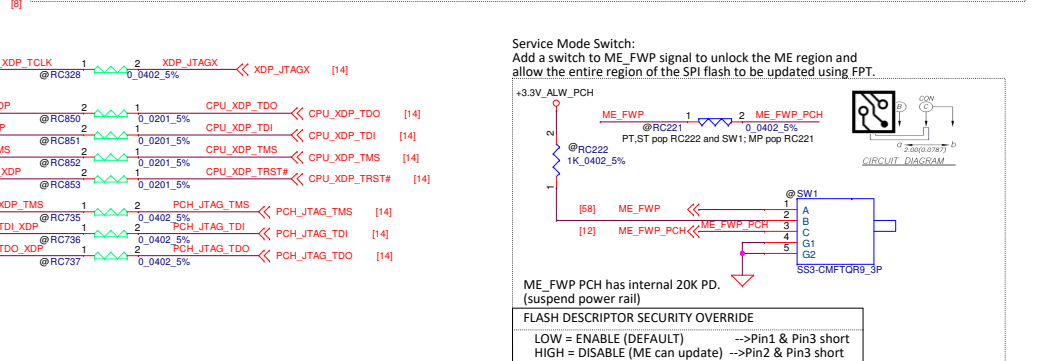
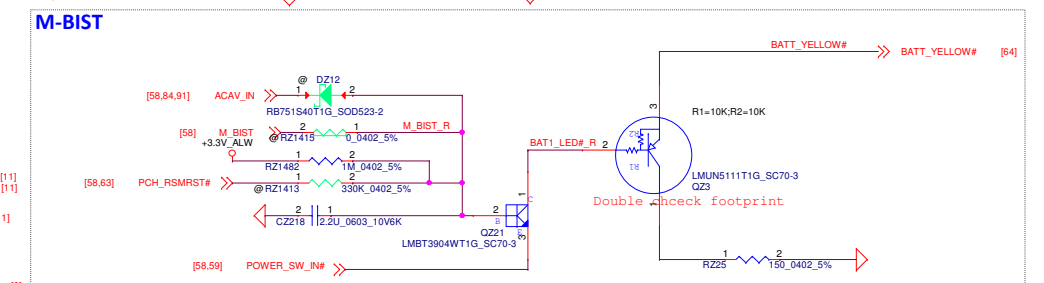
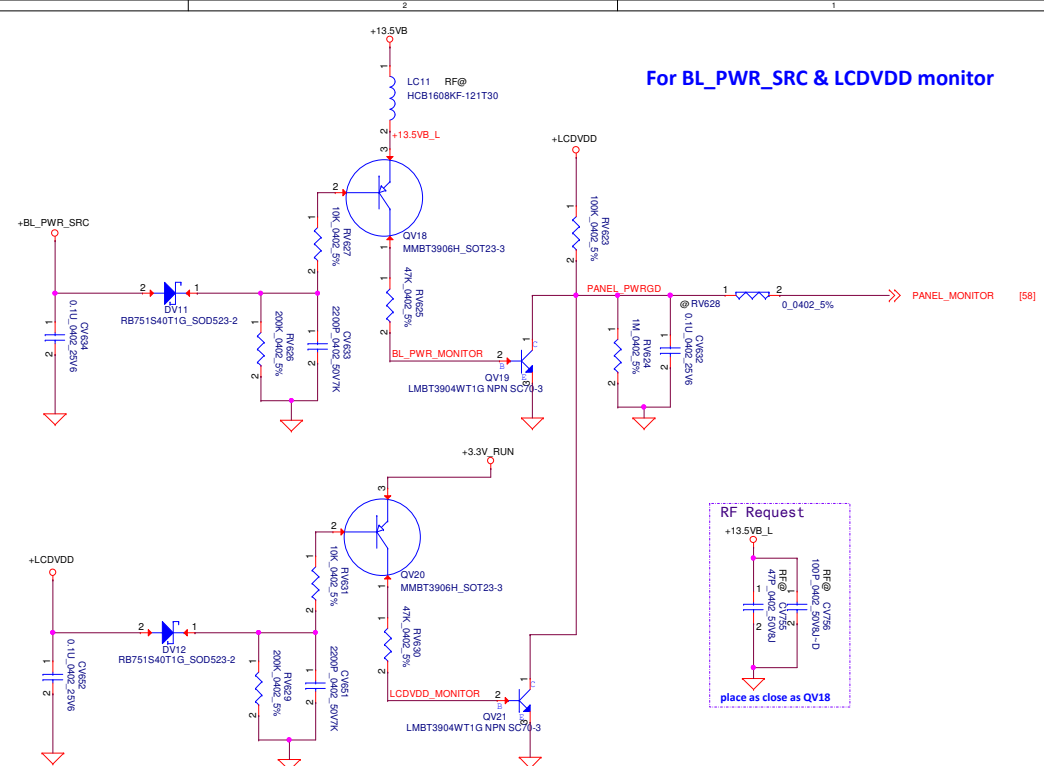
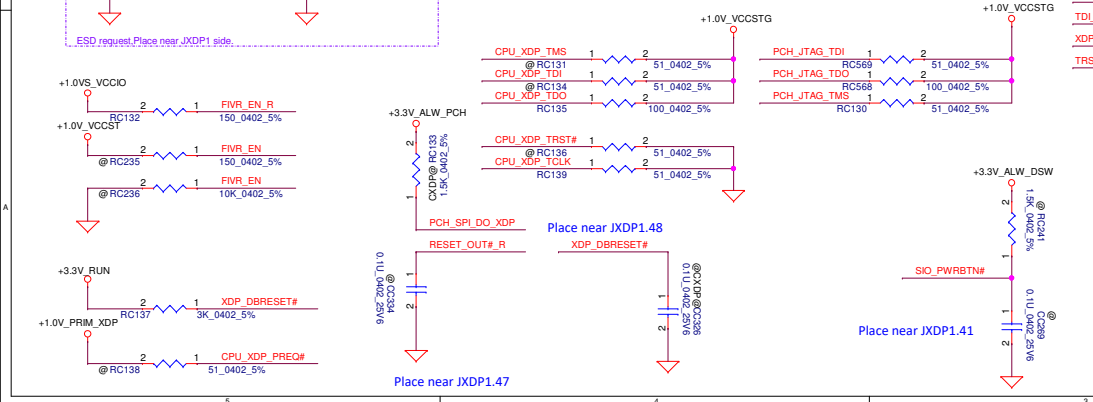
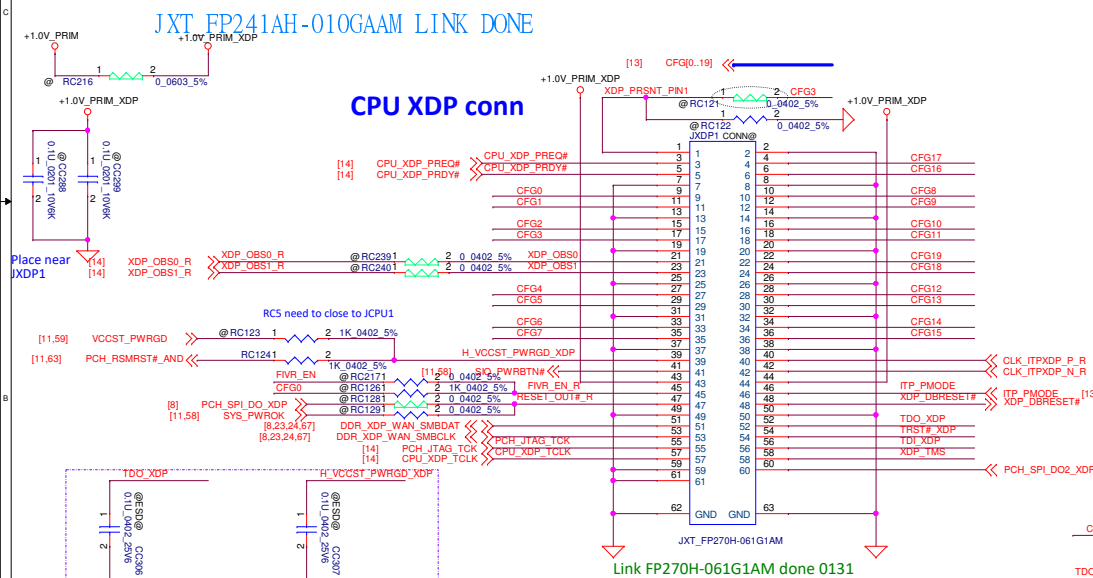
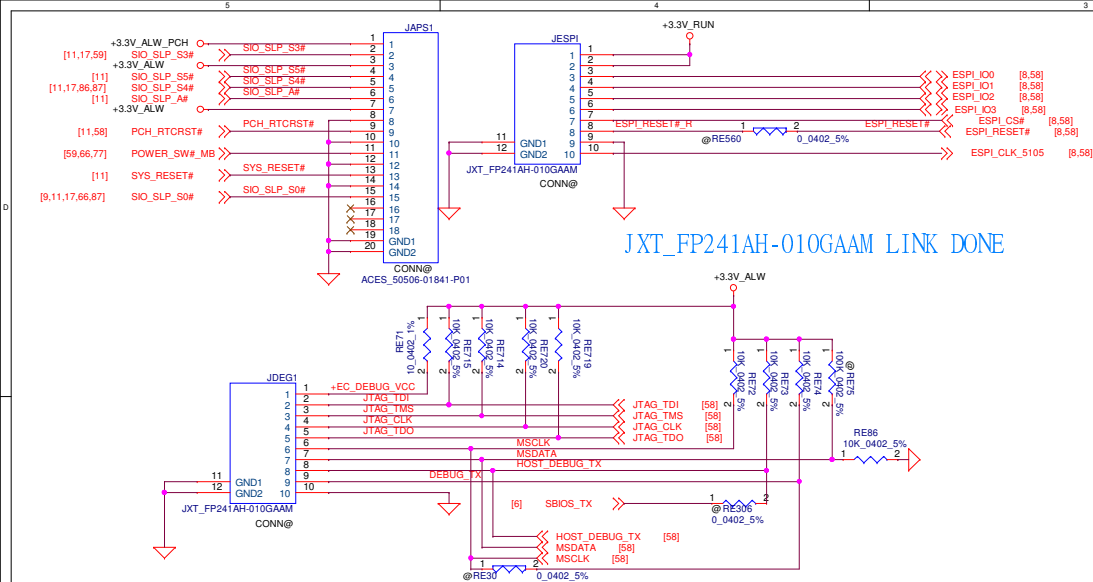
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Title		Power control	
Size	Document Number	Rev 0.3	
Date: Monday, February 25, 2019		Sheet 78	of 102

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Compal Electronics, Inc.

XDP/CMC/APS...debug

LA-G891P

File: _____

Size: _____ Document Number: _____ Rev: 0.3

Date: Monday, February 25, 2019 Sheet: 79 of 102

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Compal Electronics, Inc.			
Title	Google Debug		
Size	Document Number	Rev	
Date: Monday, February 25, 2019		Sheet 80 of 102	102
LA-G891P		0.3	

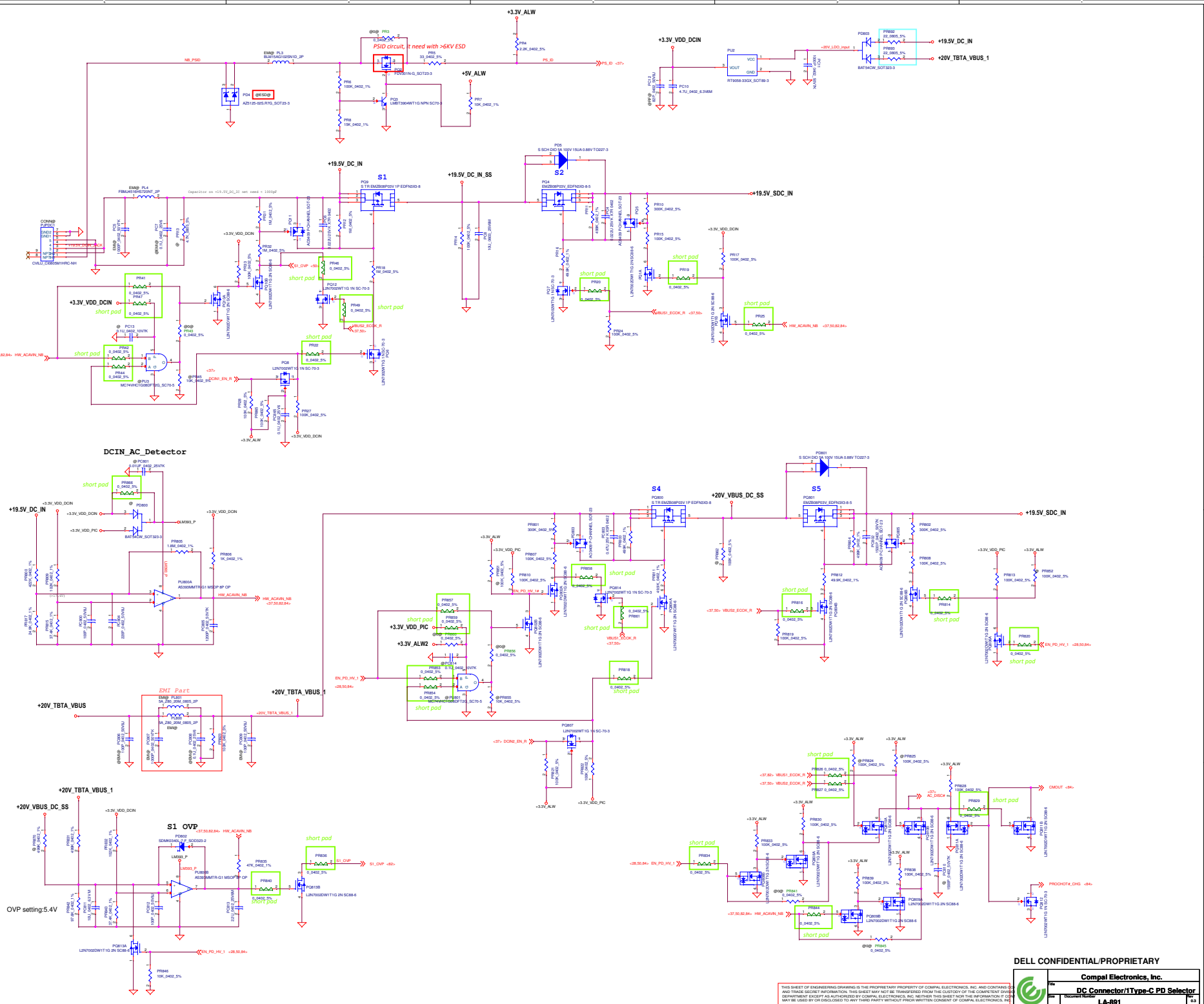


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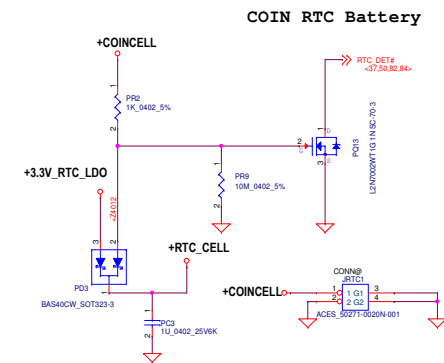
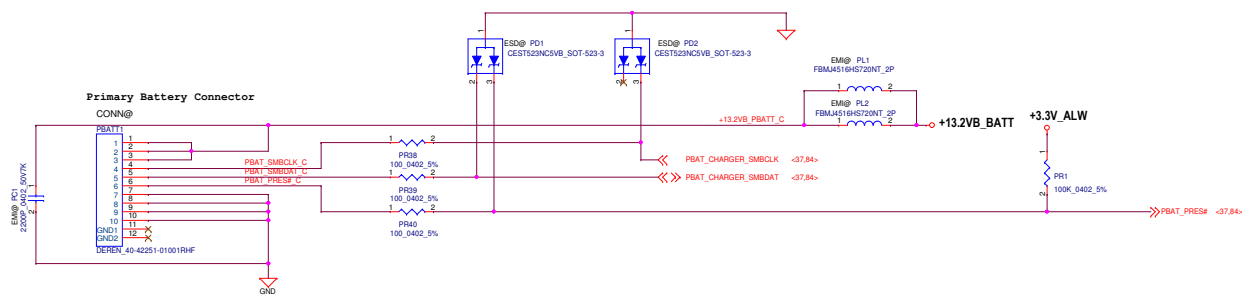
Compal Electronics, Inc.		
Title PWR-Block Diagram		
Size	Document Number LA-893	Rev 0.1
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	Compal Electronics, Inc.	
	DC Connector/1Type-C PD Selector	
	Document Number	LA-891
	Rev	Monday, February 24, 2014

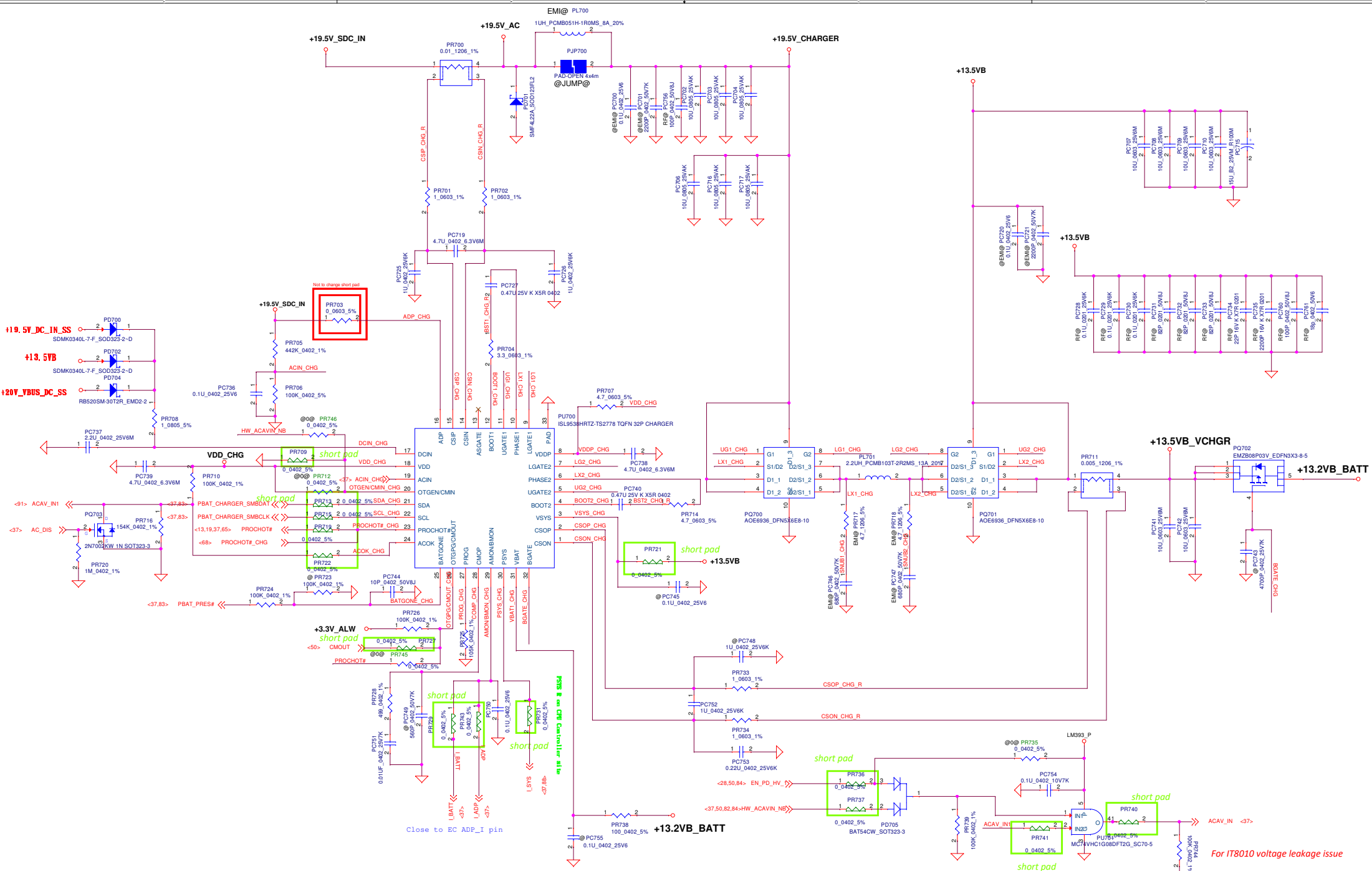
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Compal Electronics, Inc.	
Battery Connector/ RTC	
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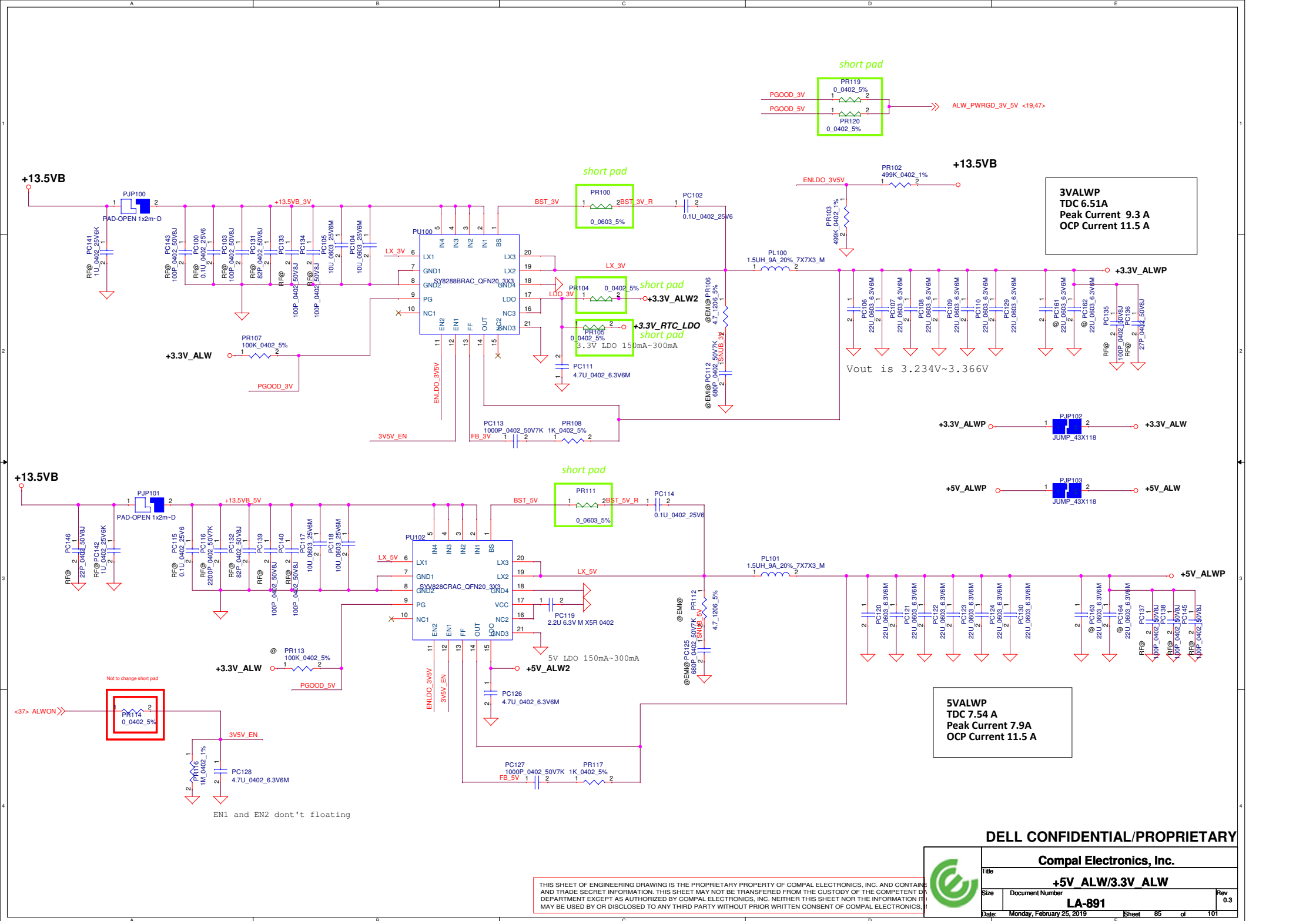
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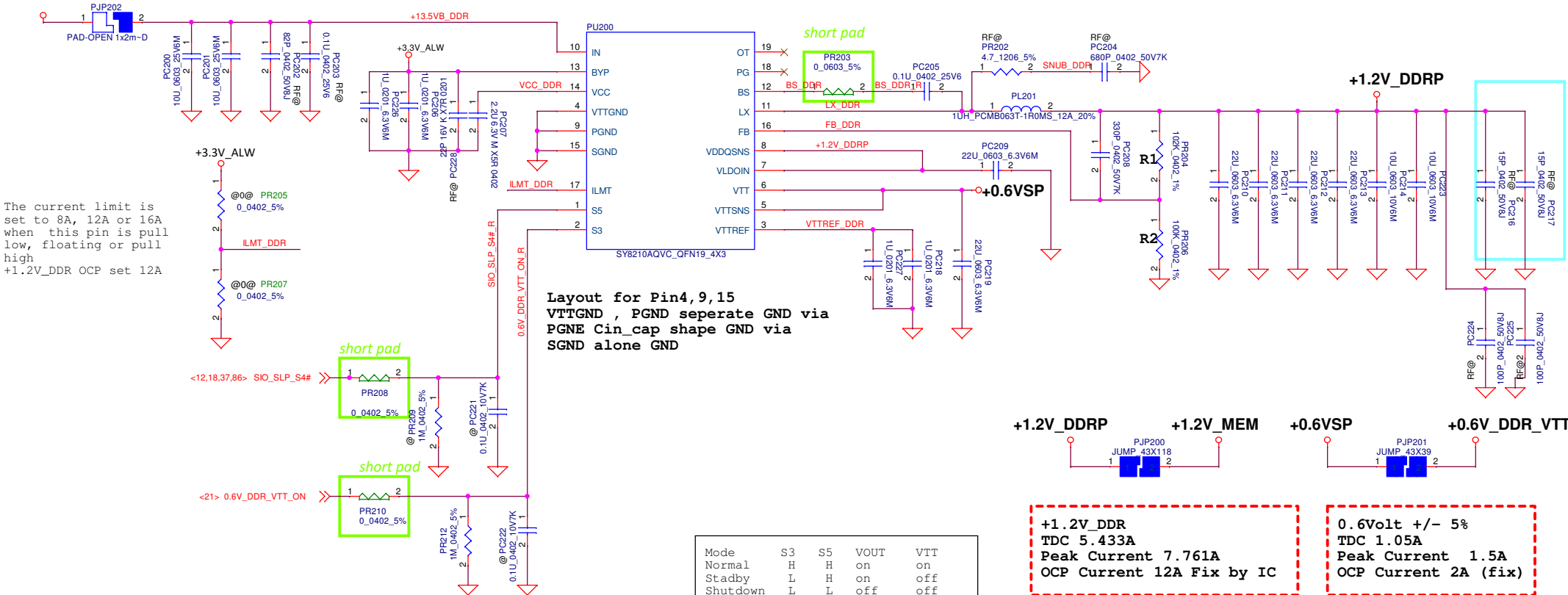
Compal Electronics, Inc.	
Charger	
LA-891	
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DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.			
Title			
+5V_ALW/3.3V_ALW			
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+13.5VB



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 12A

Layout for Pin4,9,15
VTTGND , PGND separte GND via
PGNE Cin_cap shape GND via
SGND alone GND


Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 5.433A
Peak Current 7.761A
OCP Current 12A Fix by IC

0.6Volt +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 2A (fix)

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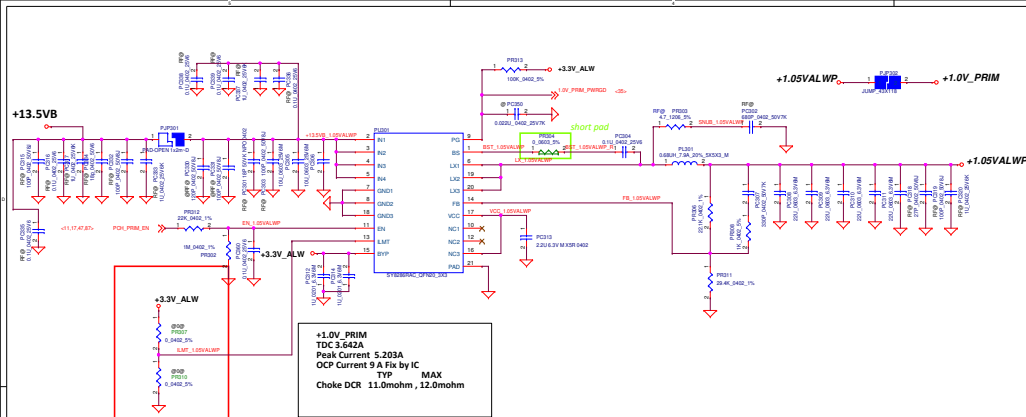
Compal Electronics, Inc.

Title
+1.2V MEN/+0.6V DDR VTT

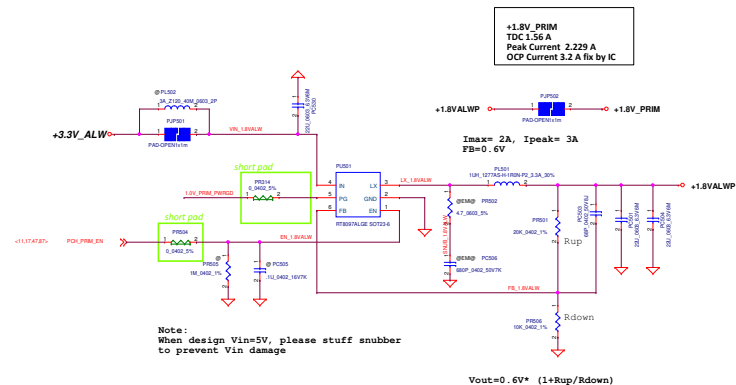
Size	Document Number	Rev
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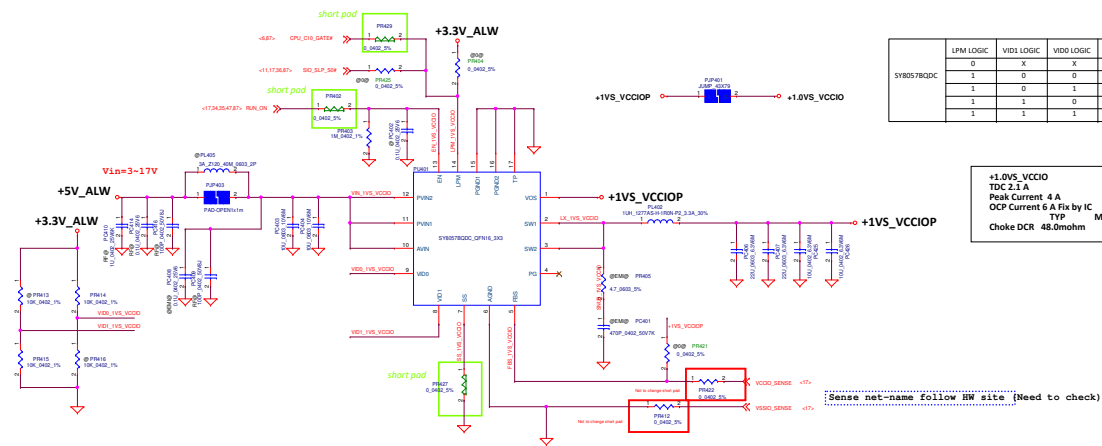
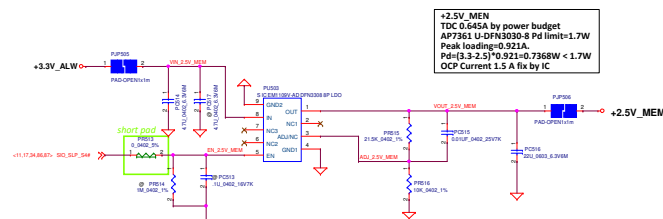
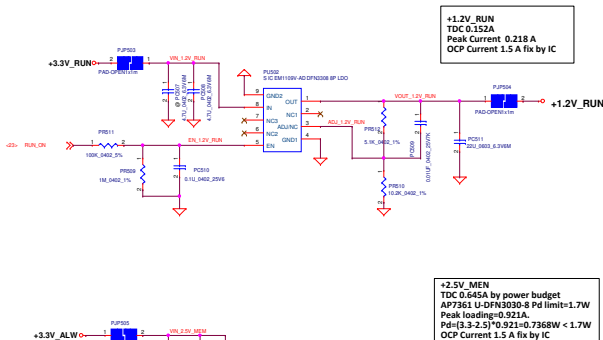


The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high.



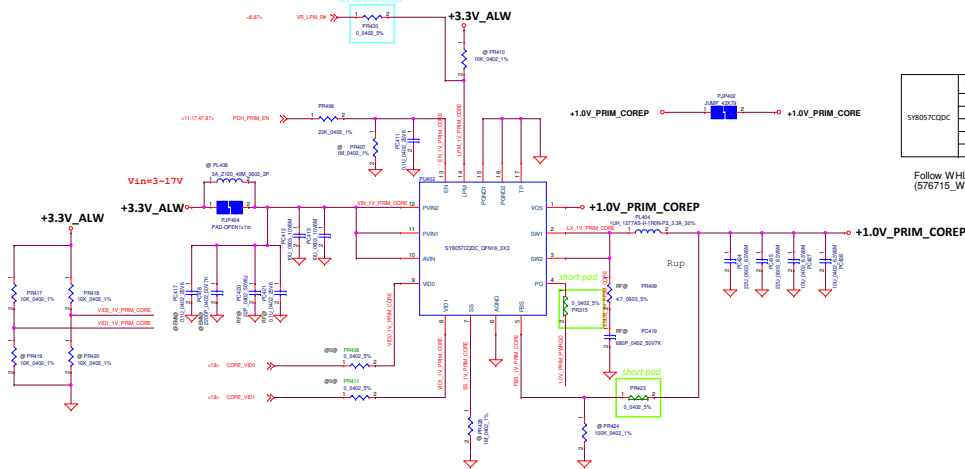
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out} = 0.6V \cdot (1 + R_{up}/R_{down})$$



	LPM LOGIC	VDD LOGIC	VDD LOGIC	OUTPUT VOLTAGE
SY8057BQDC	0	X	X	0.95V
	1	0	0	0.95
	1	1	0	1.00
	1	1	1	1.05

Sense net-name follow HW site (Need to check)

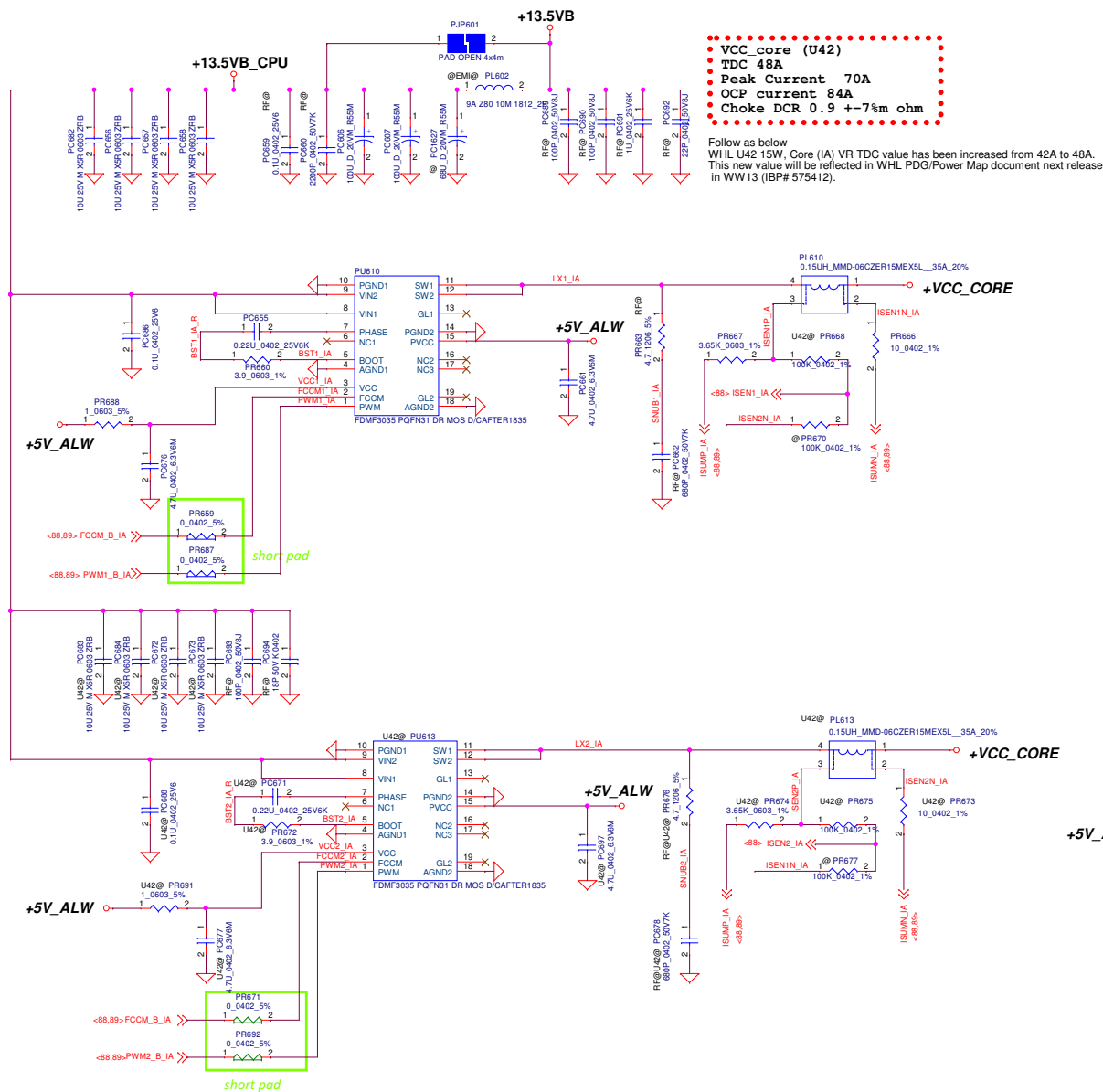


	LPM LOGIC	VDD LOGIC	VDD LOGIC	OUTPUT VOLTAGE
SY8057CQDC	0	X	X	0.75V(PM)
	1	0	0	0.9
	1	1	0	0.95
	1	1	1	1.00
	1	1	1	1.05

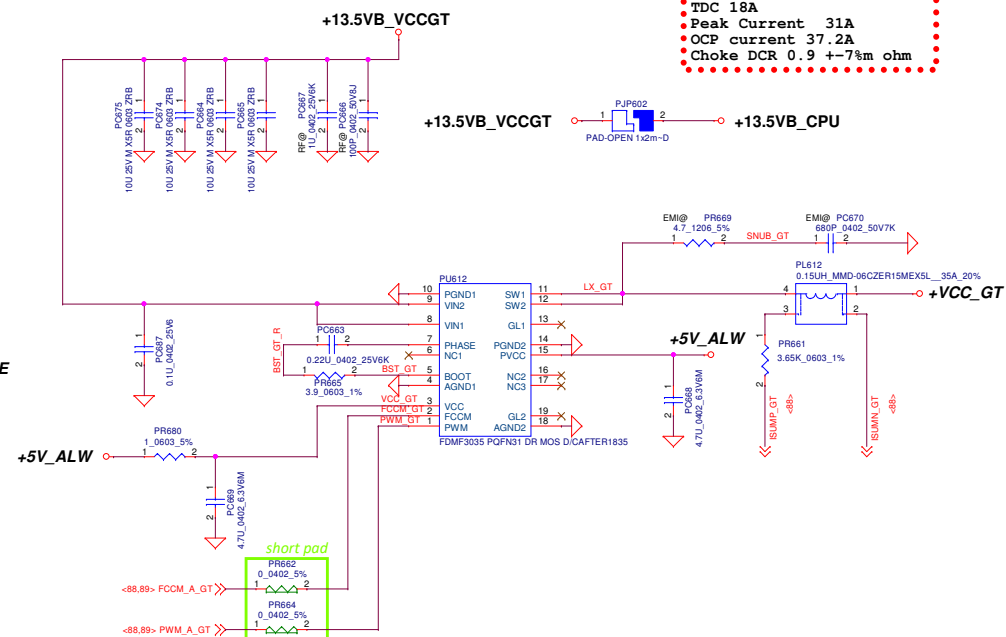
Follow WHL
(S76715_WHL_U_DDR4_HDK_HW_Design_Kit_Rev0p5)

+1.0V PRIM_CORE
TDC 2.237 A
Peak Current 3.195A
OCP Current 6.8 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

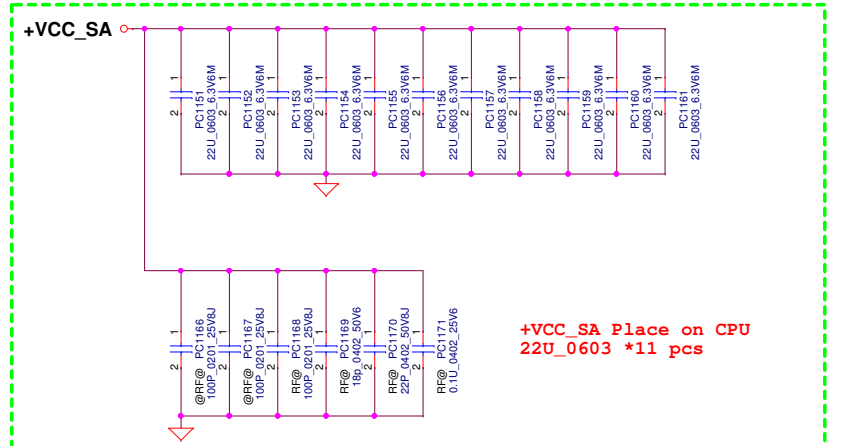
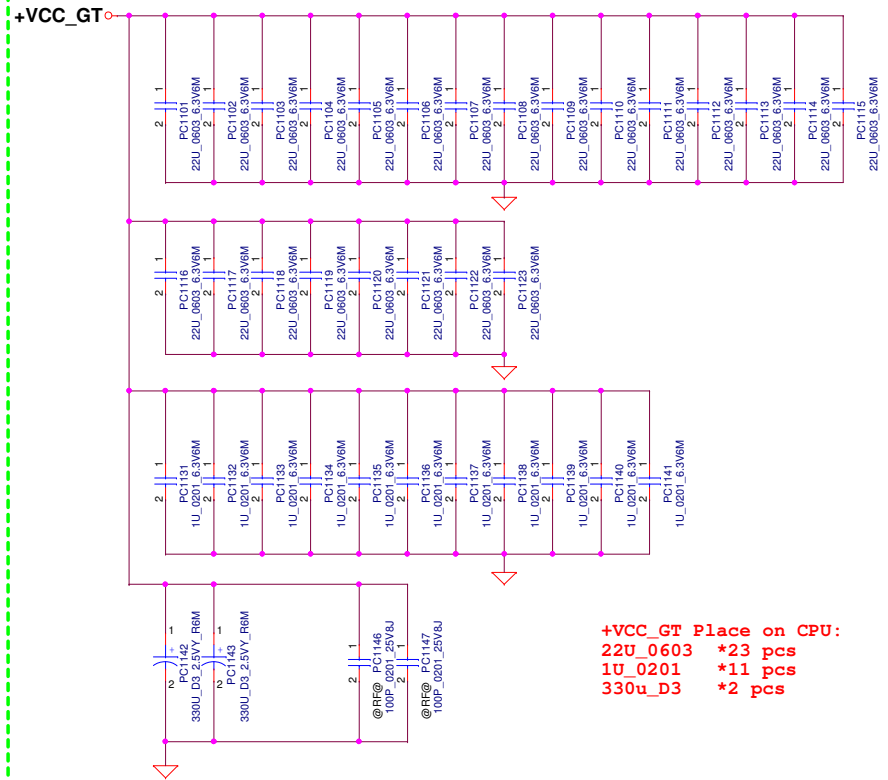
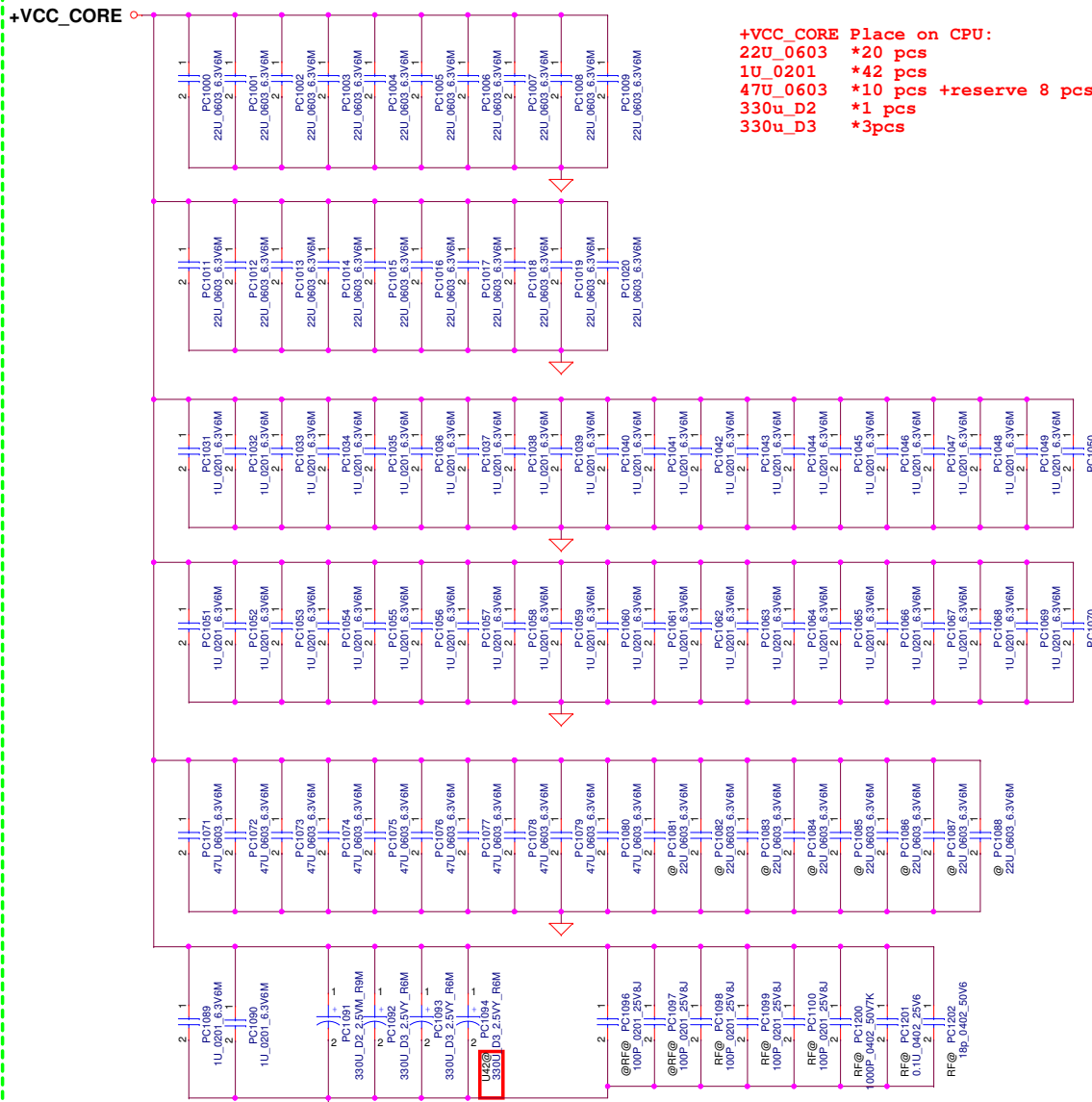
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Follow as below
 WHL U42 15W, Core (IA) VR TDC value has been increased from 42A to 48A.
 This new value will be reflected in WHL PDG/Power Map document next release
 in WW13 (IBP# 575412).



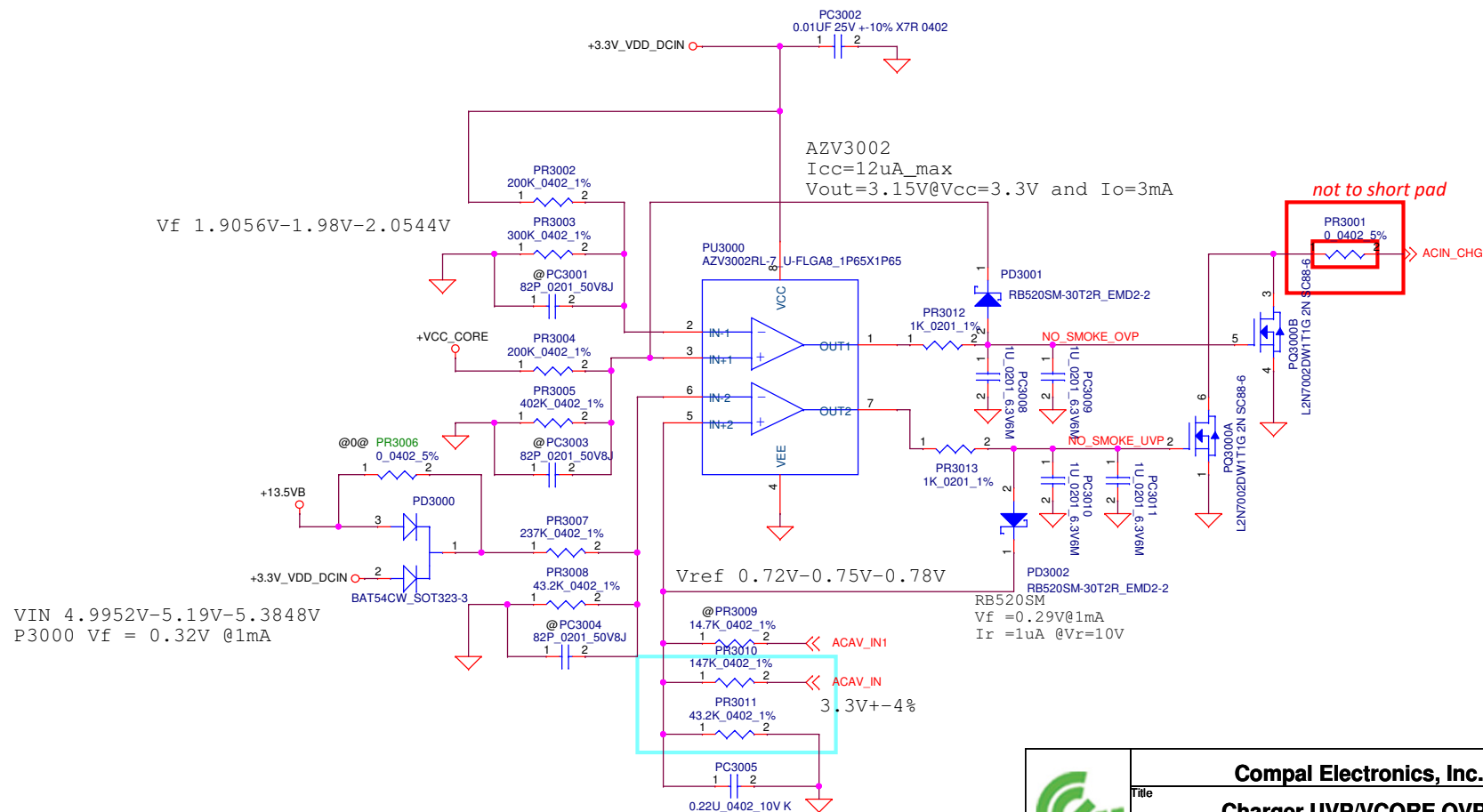
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Compal Electronics, Inc. CPU Decoupling CAP			
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VIN 4.9952V-5.19V-5.3848V
P3000 Vf = 0.32V @1mA

			Compal Electronics, Inc.	
			Charger UVP/VCORE OVP	
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
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
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



			
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U42

PC626 U42@ 	PR613 U42@ 	PR621 U42@ 	PC624 U42@ 	PC621 U42@ 
0.1U_0402_10%	97.6K_0402_1%	316_0402_1%	0.022U_0402_10%	680P_0402_10%
PR638 U42@ 	PR622 U42@ 	PC616 U42@ 	PC617 U42@ 	
523_0402_1%	2.49K_0402_1%	68P_0402_5%	1200P_0402_10%	

U22

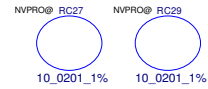
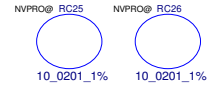
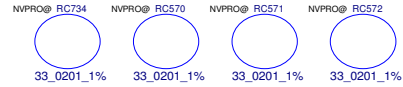
PC626 U22@ 	PR613 U22@ 	PR621 U22@ 	PC624 U22@ 	PC621 U22@ 
0.047U_0402_10%	84.5K_0402_1%	316_0402_1%	0.033U_0402_10%	820P_0402_10%
PR638 U22@ 	PR622 U22@ 	PC616 U22@ 	PC617 U22@ 	
412_0402_1%	1.65K_0402_1%	33P_0402_5%	1200P_0402_10%	

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Version Change List (P. I. R. List)						
Item	Page#	Date	Issue Description	Solution Description	Rev.	
D	1	P089	06/04	Fairchild & AOS Dr.MOS vendor remove PVCC reserved resistor	Delete reserved PR686/PR689/PR681 on PVCC side	X01
	2	P082 P086 P088 P089	06/08 07/02	Change to common PN	1. PC624 change to SE076223K80 (S CER CAP 0.022U 16V K X7R 0402) 2. PC604 change to SE074221K80 (S CER CAP 220P 50V K X7R 0402) 3. PC633 change to SE075472K80 (S CER CAP 4700P 25V K X7R 0402) 4. PL201 change to SH00000YB00 (common P/N) 5. PL614 change to SH00001ED00 (common P/N)	X01
	3	P090	07/12	Merion Top side Z-height limitation	1. Un-stuff PC1094 (U428) 2. Add stuff PC1095 - 330uF (Bottom side)	X01
	4	P088 P099	07/13	CPU tune value by intersil	1. Change the PR636 from 665 Ohm to 634 Ohm. - (VCCSA R1) -> SD000002280, S RES 1/16W 634 +-1% 0402 2. Change the PR640 from 374 Ohm to 365 Ohm. - (VCCGT R1) -> SD034365080, S RES 1/16W 365 +-1% 0402 3. Change the PC646 from 0.047uF to 0.0022uF. - (VCCGT RC) -> SE075222K80, S CER CAP 2200P 25V K X7R 0402 4. Change the PC642 from 0.033uF to 0.068uF. - (VCCGT RC) -> SE000003380, S CER CAP 0.068U 16V K X7R 0402 5. Change the PC621 from 680pF to 820pF. - (VCC1A FB RC). -> SE000008980, S CER CAP 820P 25V K X7R 0402 6. Change the PR611 from 1.87kOhm to 9.31kOhm. - (PROG2) -> SD034931180, S RES 1/16W 9.31K +-1% 0402	X01
C	5	P082 P083	07/20	ESD request	PD1, PD2, change to SCA00002A00 for ESD demand	X01
	6	P082	07/30	LPS function test fail on G3 mode. Need to return LDO(PU2) design circuit.	Need stuff item : PU2/ PC10/ PC11/ PR47/ PR33/ PR27/ PR17/ PD800 / PR806 / PR809/ PR832/ PR859 / PR810 / PR813 Need delete location : PR48 / PR34 / PR35 / PR36 / PR37/ PR847 / PR848 / PR849/ PR850 Need un-stuff item : PR851 / PR860 / PR852	X01
	7	P082	07/30	PQ8 gate for non-Backdrive issue	Add R/C delay PR865/PC865 : 100K(SD028100380) and 0.1uF_0402_25V(SE00000G880)	X01
	8	P082	08/10	LM393 resistor value fine tune	PR800 change to 422K_0402_1% (SD034422380) PR815 change to 37.4K_0402_1% (SD034374280) PR832 change to 102K_0402_1% (SD028102380) PR843 change to 37.4K_0402_1% (SD034374280) PR831 change to 1M_0402_1% (SD034100480) PR842 change to 191K_0402_1% (SD034191380)	X01
	9	P088	08/10	ISL95857C solution	PR651 value change to 39.2K for ISL95857C	X01
	10	ALL	08/10	Intel validation tune value by Intersil FAE	Change the PR629 from 90.9kOhm to 86.6kOhm. IMON of GT Change the PR636 from 665 Ohm to 634 Ohm. R1 of SA Change the PR651 from 78.7kOhm to 39.2kOhm. IMON of SA. Change the PR611 from 1.87kOhm to 9.31kOhm. PROG2 Change the PC646 from 2200pF to 6800pF. Cn of GT.	X01
	11	P082 P083	08/15	Follow Schematic naming rule	Re-define the RTC/DCIN/Battery connector from 8 to CONN8.	X01
	12	P082 P083	08/15	Check and modify connector P/N	PJPDC1 - SP02001A500 PBATT1 - SP02001A700 JRTC1 - SP02000R000	X01
	13	P087	08/15	R/C delay fine tune for WHL bring up sequence	1. Modify PR312 / PR406 value from 0 ohm to 22K_0402_1% (SD034220280) 2. PC411 change to stuff 3. Add PC360 : 0.1uF_0402_25V (SE00000G880)	X01
	14	P091	08/20	Remove double pull down resistor	Un-stuff PR505 / PR407	X01
B	15	P083	08/21	RTC issue	Add RTC detect circuit 1. Add PR9 10Mohm 2. Add PQ13 MOS	X01
	16	P091	08/22	Smokeless circuit for Vcore	Add smokeless circuit for Vcore	X01
	17	P082	08/22 09/11	LPS function modify	1. Add un-stuff PR870 and pull up source is +20V_VBUS_DC_SS ; 499K_0402_1% (SD034499380) 2. Modify PR831 value to 499K_0402_1% (SD034499380) and pull up source change to +20V_TBTA_VBUS_1 3. Modify PR842 value to 97.6K_0402_1% (SD034976280) 4. PC811 change to SE00000UD00 (10U 6.3V M X5R 0402)	X01
	18	P082	08/22	Modify 1 barrel / 1 Type-C External LDO circuit for No Smoke design	1. PD800 change to un-stuff 2. Add PR866 0_0402_5% 3. Add PD803 (BAT54CW_SOT323-3) 4. Add un-stuff PR868 0_0603_5%	X01
A	19	P088 P089	08/22	CPU VR input Low noise MLCC PCB footprint update : C_0603-S3	IA input : PC658 / PC657 / PC656 / PC682 / PC683 / PC684 / PC672 / PC673 GT input : PC675 / PC674 / PC664 / PC665 SA input : PC612 / PC608 IA output : PC1071 / PC1072 / PC1073 / PC1074 / PC1075/ PC1076 / PC1077 / PC1078 / PC1079 / PC1080	X01
	20	P090	08/22	Un-stuffed CPU +VCC_CORE output MLCC change value	Change reserve location from 47uF to 22uF (Keep un-stuff) PC1081 / PC1082 / PC1083 / PC1084 / PC1085 / PC1086 / PC1087 / PC1088	X01
	21	P089	08/22	Remove double net name	Remove PU610 / PU612 / PU613 Dr.MOS pin 15(PVCC) double net name	X01
	22	P087	08/23	Change PU301, PU501 powergood connection netname	Change connection to 1.0V_PRIM_PWRGD from 1.8V_PRIM_PWRGD (PU301, PU501)	X01
	23	P087	08/28	R/C for WHL sequence	1. Add PR313 : 100K_0402_5% 2. Add PR314 / PR315 : 0 ohm 3. Reserve PC350 footprint to PG (1.0V_PRIM_PWRGD) signal	X01
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SENSOR

LA-G891P

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Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil	Delay time (ps/inch)	35 ± 3.5 ohm single-end	40 ± 4 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm Single-end	52 ± 5.2 ohm Single-end	80 ± 8 ohm Diff.	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	85 ± 8.5 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	90 ± 9 ohm Diff.	100 ± 10 ohm Diff.	Ref
			SolderMask	GA-150LL	0.50		trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	
			Add Plating		0.95								SE50			SE 50			SE50		
1	Top		Copper foil	0.5oz	0.65	145.30	8.1	6.6	5.3	4.2	3.9	4.4/3.5	4.2/3.1	4/3.5	3.8/3.5	4.2/4.2	3.5/3.6	3.5/3.9	4.2/5.8	3.5/7.1	L2
		3.7	Prepreg	1086 or 1060	2.65		35.3	39.94	44.57	50.16	51.84	80.13	80.31	83.26	84.93	84.93	88.19	89.84	90.14	99.93	
2	GND/PWR		Copper foil	1oz	1.25																
		3.8	Core	3mil	3.00								SE50			SE 50			SE50		
3	Sig1		Copper foil	1oz	1.25	161.68	7.5	6	4.8	3.9	3.6	4/3.5	3.9/3	3.7/3.5	3.5/3.6	3.9/4.4	3.5/4.2	3.5/4.7	3.9/5.6	3.5/9.6	L2/L4
		3.7	Prepreg	7626+1080	10.95		35.29	40.13	45.06	49.72	52.16	80.22	80.68	85.65	85.01	85.09	87.98	90.04	90.53	99.97	
4	GND/PWR		Copper foil	1oz	1.25																
		3.8	Core	3mil	3.00								SE50			SE 50			SE50		
5	Sig2		Copper foil	1oz	1.25	162.52	7.8	6.3	5	4	3.6	4/3.5	4/3	3.7/3.5	3.5/3.6	4/4.6	3.5/4.2	3.5/4.7	4/6	3.5/9.2	L4/L7
		3.8	Prepreg	7626+1080	10.28		35.36	39.85	44.94	49.94	52.3	80.16	80.17	82.61	84.91	84.99	87.93	90.03	90.99	99.97	
6	Sig3		Copper foil	1oz	1.25	162.52	7.8	6.3	5	4	3.6	4/3.5	4/3	3.7/3.5	3.5/3.6	4/4.6	3.5/4.2	3.5/4.7	4/6	3.5/9.2	L4/L7
		3.8	Core	3mil	3.00																
7	GND/PWR		Copper foil	1oz	1.25																
		3.7	Prepreg	1086 or 1060	2.65								SE50			SE 50			SE50		
8	Bottom		Copper foil	0.5oz	0.65	145.30	8.1	6.6	5.3	4.2	3.9	4.4/3.5	4.2/3.1	4/3.5	3.8/3.5	4.2/4.2	3.5/3.6	3.5/3.9	4.2/5.8	3.5/7.1	L7
			Add Plating		0.95		35.3	39.94	44.57	50.16	51.84	80.13	80.31	83.26	84.93	84.93	88.19	89.84	90.14	99.93	
			SolderMask		0.50																
Overall Thickness (1.2mm ± 10%)					47.23000																

1.199642

Reference GCE RD data

線寬線距<3.5mil or 線距>12mil不建議使用

40 ± 4 ohm single-end	45 ± 4.5 ohm single-end	50 ± 5 ohm single-end	52 ± 5.2 ohm single-end	80 ± 8 ohm Diff.	83 ± 8.3 ohm Diff.	85 ± 8.5 ohm Diff.	88 ± 8.8 ohm Diff.	90 ± 9 ohm Diff.	Ref	100 ± 10 ohm Diff.	Ref
trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)	trace Width (±12%)		trace Width (±12%)	
								8.5/4.5	L3	12/5	no Ref
								90.14		100.75	
										11/6.5	no Ref
										99.63	
6	4.8	3.8	3.5	4/3.5	3.7/3.5	3.5/3.6	3.5/4.2		L4/L6	10/6.5	no Ref
39.87	44.8	50.03	51.88	80.1	82.59	84.91	87.85			99.46	
6	4.8	3.8	3.5	4/3.5	3.7/3.5	3.5/3.6	3.5/4.2		L5/L7	10/6.5	no Ref
								8.5/4.5	L6	12/5	no Ref
								90.14		100.75	

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